Charge Transfer in Overlapping Gate Charge-Coupled Devices

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Abstract—**A detailed numerical simulation of the free charge transfer in overlapped gate charge-coupled devices (CCD) is presented. The transport dynamics are analyzed in terms of thermal diffusion, self-induced fields, and fringing fields under all the relevant electrodes and the interelectrode regions with time-varying gate potentials. The results of the charge transfer with different clocking schemes and clocking waveforms are presented. The dependence of the stages of the charge transfer on the device parameters are discussed in detail. A lumped-circuit model of CCD that could be used to obtain the charge-transfer characteristics with various clocking waveforms is also presented.**

I. Introduction

THE overlapping gate charge-coupled device (CCD) is presently the most technically promising structure for the potential large scale applications of these devices. Compared to the simplicity of the three-phase metal gate CCD [1], [2] and the resistive gate CCD [3], the interelectrode spacing in the overlapping gate structure is reduced to an oxide thickness and the overlapping electrodes provide good control of the surface potential in the entire channel region, seal the active channel from any external contaminations, shield out the charge repulsion,[1] and thus enhance the charge transfer. Overlapped gate CCD's can be manufactured with two levels of metallization technology such as silicon gate and refractory gate technology [4], [5]. The two levels of metallization simplify the layout of large CCD arrays. The use of the overlapping gate structure with polysilicon and aluminum electrodes in an

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[1] The maximum current that can be transferred across an inversion layer produced by a metal gate of length l and width W is given approximately by (as shown in Appendix III)

$$I \cong \frac{\mu C W}{2l} \Phi_0^2,$$

where C is the oxide capacity, μ the surface mobility, and Φ_0 is the surface potential without charge. If an inversion layer is produced by a constant normal field in a gap of length l and width W on a substrate of doping N_D then the relation between the surface potential Φ_S and surface charge q is given by

$$q = \sqrt{2\epsilon_S e N_D}\,(\sqrt{|\Phi_0|} - \sqrt{|\Phi_S|}),$$

where Φ_0 is the surface potential without charge, ϵ_S the semiconductor dielectric constant, and e the electronic charge. Then using the gradual channel approximation, it can be shown that the maximum current that can be transferred by the inversion layer under the gap is approximately given by

$$I' = \tfrac{2}{3} \frac{\mu C_D W}{l} \Phi_0^2,$$

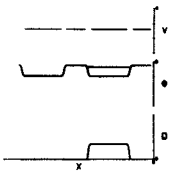
where C_D is the depletion layer capacity under the gap with no surface charge. Thus the presence of a metal gate over the inversion layer shields out the charge repulsion and increases the maximum rate of transfer of charge by the ratio of the oxide to the depletion layer capacity that is typically about an order of magnitude.

The three sequences of page-flip "movies" illustrate the dynamics of the charge transfer and charge storage in charge-coupled devices (CCD's). The frames of the movie were drawn by a SC4020 plotter directly from a numerical simulation of the charge transfer dynamics. The transport dynamics were analyzed in terms of thermal diffusion, self-induced fields and fringing fields under the relevant electrodes and interelectrode regions with various clocking waveforms. A p-channel overlapping gate CCD was used in the numerical simulation. The storage gates were 14 μ wide and 8 μ apart. In each frame the horizontal axis represents the distance along the semiconductor–insulator interface of the device. From right to left are the regions under the first transfer gate, first storage gate, second transfer gate and second storage gate of one bit of the device. The vertical axis at the bottom of the frame represents the surface charge density of the mobile carriers in normalized units. The vertical axis at the top of the frame represents the voltages applied to the storage and transfer gates (0 to −15 V). The vertical axis at the middle of the frame represents the surface potential (0 to −15 V). The upper curve is the surface potential with charge, the lower curve without charge, so the difference between the two lines is proportional to the mobile surface charge density. The time interval from one page to the next is 4 ns. The clocking waveforms and the device dimensions for the flip-page movie Sequences I, II, and III are shown at the top of Figs. 3, 4, and 7, respectively, of the paper entitled, "Charge Transfer in Overlapping Gate Charge-Coupled Devices" (this issue, pp. 191–207).

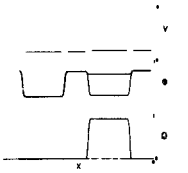
Sequence I: This flip-page movie sequence illustrates the time evolution of the surface charge density and surface potential profiles during charge transfer when a CCD is operated with a two-phase drop clock. In the two-phase clocking scheme, each successive storage and transfer gate pair is driven by one phase of the clock. The clock frequency is 5 Mc. With drop clocks the signal charge is stored under a storage gate with a holding voltage V_1(−7 V in this case). Charge transfer occurs when the voltage of the second phase of the clock driving the next transfer and storage gates is lowered to V_m (−15 V); the charge thus flows to the potential minimum created under the receiving storage gate. The charge transfer ends when the voltage of the receiving storage gate is raised to V_1.

Sequence II: This illustrates the operation of a two-phase push clock. The clock frequency is 5 Mc. With push clocks the charge is stored under a storage gate with its voltage equal to V_m (−15 V). To effect the charge transfer, the potential of the original storage gate is gradually raised, and the charge stored there begins to spill over the area beneath the next transfer gate. As the potential of the original storage gate continues to rise, more of the charge under it is brought to a potential higher than that under the next transfer gate, and so is able to flow to the next storage gate. When the potential of the original storage gate returns to V_m, the charge transfer ends, and some of the residual charge under the transfer gate spills back to the original storage gate.

Sequence III: This illustrates a CCD operating with a four-phase push clock. In the four-phase clocking scheme, the gates of each bit of the device are driven by a separate phase of the clock, thus allowing a more flexible control of the storage and transfer of the signal charge. The clock frequency is 15.4 Mc. With push clocks the charge is stored under a storage gate with its voltage equal to V_m and with the voltages of the transfer gates equal to the resting voltage V_2. For example, to transfer the charge from under the first storage gate to the second one, the voltages of the second transfer and storage gate are lowered to V_m. Then the voltage of the original storage gate increases gradually to push the charge from under the first storage gate to the adjacent ones. The second transfer gate voltage is then increased to push the charge to the second storage gate. As it reaches the resting voltage V_2, the charge transfer ends and some of the residual charge under the transfer gate spills back to the preceding storage gate.



Sequence I



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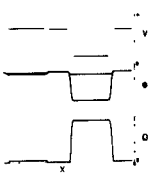


Sequence III

operating memory system has been reported recently [6].

Several authors [7]–[12] have reported studies of the free charge transfer for a model consisting of a single gate to which a time independent potential is applied and assuming a perfect sink at the end of the gate.

The purpose of this work is to study in detail the limitations on the performance of the overlapping gates CCD's due to incomplete charge transfer and interface state trapping [1], [13] and their dependence on the device parameters and the clocking waveforms. Therefore we have developed a detailed numerical simulation of the charge-transfer process in the overlapping gate CCD's. We have analyzed the charge transport dynamics in terms of charge motion due to thermal diffusion, self-induced drift, and fringing fields. With some assumptions and approximations, which are shown to be well satisfied, we have solved the nonlinear nonlocal equations describing the transfer dynamics, under all the relevant gate electrodes and interelectrode regions with time-varying gate potentials using a new finite difference scheme, the box scheme [14]. We also discuss in this paper the dependence of the different stages of the transfer process on the device parameters. Using a lumped-circuit model of CCD's, analytic expressions describing the charge transfer with various clocking waveforms are developed. These expressions can be used to derive the charge-transfer characteristics for other device structures, dimensions, clocking waveforms and voltages, thus providing practical charge-coupled device and circuit design tools. The influence of clocking waveforms and clocking schemes on incomplete free charge transfer and the effects of trapping in interface states in overlapping gate CCD's are discussed by the authors in detail elsewhere using the results of the present study [15]–[18], [26].

In Section II we discuss the theoretical model and the basis of our approximations. In Sections III and IV we present the results of the charge transfer in two-phase and four-phase CCD's. A discussion of the results is presented in Section V.

II. Theoretical Model

In the calculations presented here we have considered p-channel[2] devices with dimensions consistent with typical layout tolerances of silicon gate technology.

Transport Equations

The storage and transfer of charge along the insulator-semiconductor interface is described by the continuity equation:

$$\frac{\partial q}{\partial t} = \frac{-\partial}{\partial x} J_x - \frac{\partial q}{\partial t}\bigg|_{\text{trapping}} + \frac{\partial q}{\partial t}\bigg|_{\text{thermal generation}}, \tag{1}$$

where

$$J_x = -D\frac{\partial q}{\partial x} - \mu q \frac{\partial \Phi_s}{\partial x}. \tag{2}$$

q is the surface-charge density of the free minority carrier, J_x the sheet current density, and Φ_s the surface potential. D and μ are the minority carrier diffusion and mobility at the interface, respectively. x is the distance along the interface in the direction of charge transfer.

$$\frac{\partial q}{\partial t}\bigg|_{\text{thermal generation}}$$

is the rate of generation of surface charge due to thermal generation currents from generation centers at the interface, the depletion regions, and the substrate. For a total delay time from the input to the output of the device much smaller than the storage time of the interface, the effect of thermal generation can be neglected.[3]

$$\frac{\partial q}{\partial t}\bigg|_{\text{trapping}}$$

is the total rate of capture of the mobile carriers due to their interaction with the interface states in the band gap. Since the mobile carriers interact with interface states within an energy range of the order of thermal voltage and for the low interface state density obtainable with the present thermally grown silicon oxide, the rate of capture or emission of the mobile carriers by the interface states is smaller than the divergence of the sheet current density in (1) [15]. Thus one can obtain the free charge-transfer characteristics by neglecting

$$\frac{\partial q}{\partial t}\bigg|_{\text{trapping}}$$

in (1) and solving the continuity equation. The effects of trapping on the incomplete charge transfer can then be calculated by studying the interaction of the mobile carriers with the interface states from the Shockley–Read–Hall equations together with the surface-charge density profiles $q(x, t)$ under the gates [15]. Thus the free charge-transfer continuity equation reduces to

$$\frac{\partial q}{\partial t} = \frac{\partial}{\partial x}\left[D\frac{\partial q}{\partial x} + \mu q \frac{\partial \Phi_s}{\partial x}\right]. \tag{3}$$

The surface-potential gradient $\partial\Phi_s/\partial x$ is due to the variable surface-charge density and the two-dimensional nature of the CCD structure. For given electrode potentials, device geometry, and charge density profile, the surface-potential gradient is obtained from the solution of the two-dimensional Poisson equation. Thus a rigorous treatment of the free charge-transfer problem would require the simultaneous solution of (3) and the two-dimensional Poisson equation. While this rigorous approach is conceptually possible, the cost of such an analysis leads us to seek some valid approximation to simplify the solution.

The surface-potential gradient due to variations in the surface-charge density (self-induced fields) can be obtained, according to the standard gradual channel approximation [20]. In this approximation, we take the gradient of the surface potential Φ_s obtained from the one-dimensional solution of the Poisson equation with the parameters of the solutions chosen to cor-

[2] The calculations and results can be applied to n-channel devices after the proper scaling of the transfer times by the surface mobility ratio of the electrons and holes and the use of the appropriate values of the threshold and flat-band voltages.

[3] Thermal generation and leakage currents impose a limit on the maximum delay time and the minimum clock frequency of the device. For more detailed discussion see [17]–[19].

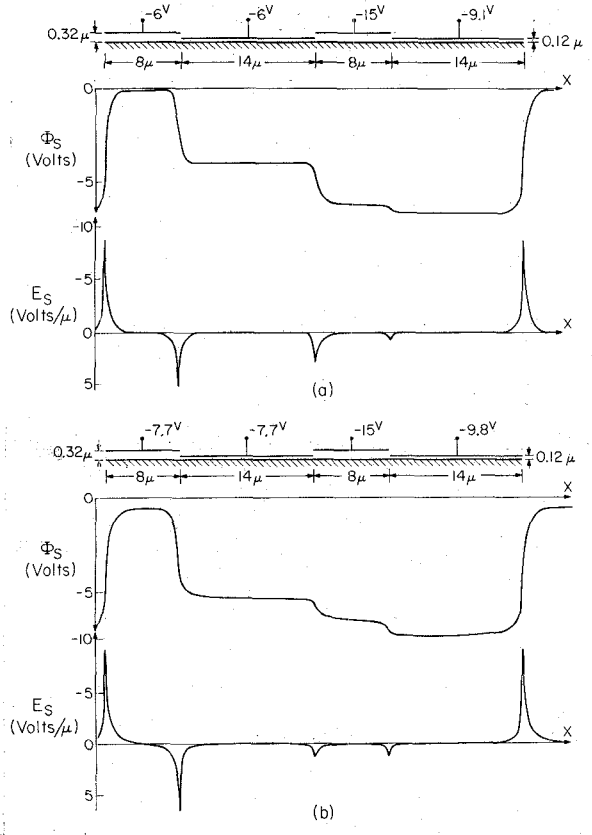


Fig. 1. Plots of the surface potential and surface-potential gradient along the silicon–silicon oxide interface obtained from the solution of the two-dimensional Poisson equation of the overlapping gate structure in Fig. 1 with minimum geometry dimensions. The thickness of the polysilicon and the aluminum electrodes is 0.5 μ. The electrode voltages correspond to the last stages of the charge transfer. A signal charge of about 5.5 V is in the receiving storage electrode. The substrate doping is 8×10^{14} donors/cm^3 in Fig. 1(a) and 10^{14} donors/cm^3 in Fig. 1(b).

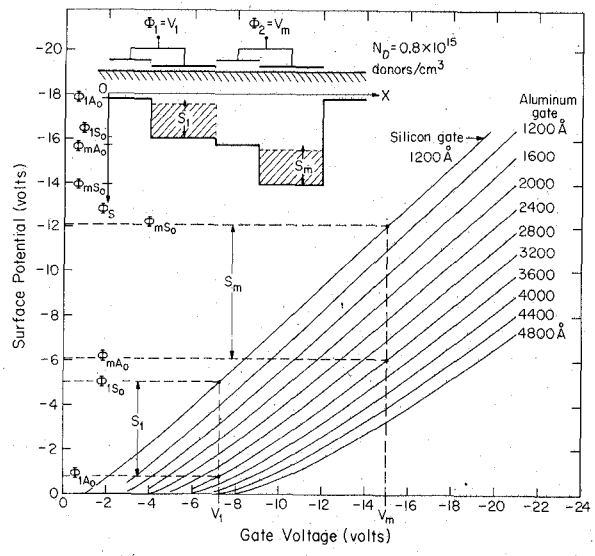


Fig. 2. Plots of the one-dimensional relation between the surface potential Φ_s and the gate voltage for a polysilicon gate with 1200 Å and aluminum gates with different oxide thickness. The substrate doping is 0.8×10^{15} donors/cm^2. $q_{ss} = 3.1 \times 10^{11}$/cm^3.

respond to the one-dimensional cut through the structure. In Appendix I we show, using a Green's function solution of the two-dimensional Poisson equation for an arbitrary minority charge density profile, that the gradual channel approximation is reasonably accurate when the lateral variation of the various charges over a distance on the order of the depletion layer width is small.

The surface-potential gradient under the electrodes due to the adjacent electrodes (fringing fields) is obtained by solving the two-dimensional Poisson equation of the CCD structure. In Fig. 1 we have plotted the surface potential and surface-potential gradient along the semiconductor insulator interface. These plots were obtained from the solution of the two-dimensional Poisson equation [21] of an overlapping gate CCD with the electrode voltages corresponding to the last stages of the charge transfer and with most of the signal charge in the receiving storage electrode. The fringing fields in devices with dimensions consistent with typical layout tolerances of MOS technology, are of the order of a few hundreds volts/centimeter. During the first stages of the charge-transfer process the self-induced fields are typically few thousands volts/centimeter, therefore, the fringing fields are only important at the last stages of the charge transfer when the self-induced fields become very small. Accordingly, the fringing-field profile under the electrodes obtained from a two-dimensional solution of the Poisson equation of the CCD structure with the gate voltages corresponding to the last stages of the charge transfer and with most of the signal charge in the receiving electrode can be used during the entire charge-transfer process.

The two-dimensional solution of the Poisson equation for the overlapping gate structure shown in Fig. 1 illustrates that the surface potential under the interelectrode regions varies quite smoothly for different gate electrode potentials [5], [21]. Therefore we have used a smooth interpolating polynomial to approximate the surface potential in these regions. We have also assumed a constant surface mobility to simplify the solutions of the transport equations. The dependence of the surface mobility on the normal surface field and the surface-potential gradient along the interface introduce negligibly small error on the charge-transfer characteristics of typical minimum geometry devices.[4]

Nonlinear Diffusion Equation

In Appendix II, we show that according to the previously mentioned assumptions the surface-potential gradient under the gates or in the interelectrode regions

[4] Carrier mobilities at the Si–SiO_2 interface are approximately constant up to a normal surface field of 1.5×10^5 V/cm corresponding to a surface carrier concentration of 10^{12}/cm^2 [22]. Therefore, for mobile carrier concentration equal or less than 10^{12}/cm^2, the reduction in the surface mobility due to the normal surface field is small. The carrier velocity in silicon saturates at a critical field around 5 V/μ [23]. During the charge transfer, the surface-potential gradient usually does not exceed 1 V/μ except in the interelectrode region between the transfer gate and the receiving storage gate, where it may reach about 10 V/μ. Since the maximum sheet current density is about few microamperes/micron, and the mobile carrier concentration in this region is smaller by more than an order of magnitude than that under the gate electrodes, the changes in the mobile carrier concentration in this region due to velocity saturation has negligible effects on the charge-transfer characteristics.

can be written in the form

$$\frac{\partial \Phi_s}{\partial x} = L(x, t) + M(x, t)q + N(x, t)\frac{\partial q}{\partial x}. \quad (4)$$

Substituting in (3), the continuity equation reduces to the nonlinear diffusion equation

$$\frac{\partial q}{\partial t} = \frac{\partial}{\partial x}\left[D\frac{\partial q}{\partial t} + \mu q\left(L + Mq + N\frac{\partial q}{\partial x}\right)\right]. \quad (5)$$

If fringing fields under the gate electrodes are negligible then $L = M = 0$.

The dynamics of the charge transport in each bit are thus described by equations similar to (5) with the appropriate functions, L, M, and N under the storage and transfer electrodes and the interelectrode regions. At the junction points between the different regions, the surface potential, and surface-charge density must be continuous and the current must be conserved.

We have solved the set of nonlinear equations with the appropriate boundary conditions using a new finite difference scheme, the box scheme [14]. The numerical formulation of the problem[5] and its accuracy is treated in detail in [18].

Overlapping gate CCD's can be operated with four-phase, three-phase, two-phase, and single-phase clocking schemes. With three-phase and four-phase clocking schemes the gate electrodes are equal in size so that charge may be stored under each gate during the transfer process. Alternatively the upper electrodes may be made smaller and used to control the transfer of charge between the buried storage electrodes. In this case, four-phase, two-phase, and single-phase clocking schemes may be used to control the storage and transfer of charge for both serpentine and parallel signal flow.

III. Two-Phase Clocking Scheme

In the two-phase clocking scheme only two clock phases are used to control the storage and transfer of charge along the interface. The asymmetry in the surface potential needed to provide the directionality of the signal charge transfer can be achieved by using a step in the channel oxide [5] or ion implanted barrier [24] or the charge storage properties of double dielectric structures such as the MNOS structures [25]. In this section we present some of the calculations of the charge-transfer characteristics of two-phase overlapping gates CCD's where the asymmetry of the structure is achieved by a step in the channel oxide. However our results can be applied to all other structures with the appropriate modifications.

Complete Charge-Transfer Mode

In the complete charge-transfer modes the charge under the storage gate is transferred to the following gates; none is deliberately retained.

[5] The box scheme has very desirable features that made it suitable for solving the set of nonlinear diffusion equations describing the charge transport dynamics in CCD. For example, second order accuracy can be achieved with nonuniform nets. Thus small net spacing can be used in the interelectrode regions where the surface-charge density is changing rapidly, while a large net spacing can be used in the other regions where the surface-charge density gradient is small. Also both the surface-charge density and its gradient are approximated with the same accuracy. Thus the charge flow across the boundaries between the different regions is conserved to the same order of accuracy of the surface charge under the electrodes.

Drop Clock: With drop clock the signal charge is stored below a gate at a holding voltage V_1 that is a fraction of the largest clock voltage V_m that the MOS structure can tolerate; charge transfer occurs when V_m is then applied to the adjacent gates and the charge flows to the potential minimum thus created [26].

In Fig. 2 we have plotted the one-dimensional relation between the surface potential and the gate voltage for a polysilicon gate with 1200-Å oxide and for an aluminum gate with different oxide thickness for a substrate doping of 8×10^{14} donors/cm^3. Since in the two-phase clocking scheme the surface potential under each successive set of transfer and storage gates is controlled by a single-clocking voltage, the maximum amount of charge that can be stored under the storage gate without spill over and the fringing fields under it depend on the silicon oxide thickness under the transfer and storage gates. Therefore, for optimum operation of the device, the oxide thickness under the storage and transfer gates should be properly chosen.[6]

We have simulated numerically the charge-transfer characteristics for the device shown at the top of Fig. 3 clocked by square-wave drop clocks with zero fall and rise times.[7] In Fig. 3 we have plotted the residual charge under the source storage gate as a percentage of a full bucket[8] for two different initial charges equivalent to about 3 V and 1 V with a substrate doping of 8×10^{14} donors/cm^3 and 10^{14} donors/cm^3. Consideration of the transient currents at the ends of the transfer gate and the surface-charge and surface-potential profiles[9] under the gates during the charge transfer show that the charge transfer divides naturally into several distinct stages.

1) In the first stage, the charge initially confined under the source storage gate spreads to charge up the adjacent transfer gate for a fraction of a nanosecond.

2) In the second stage, the charge transfer is limited by the transport of charge across the transfer gate to the next storage gate. The transfer gate acts as a MOS transistor at pinchoff with the storage gates as its source and drain. Thus the source and receiving storage gates are capacitors charged and discharged through the transfer channel.

According to the lumped-circuit model discussed in Appendix IV the decay of the residual charge under the gates is described by

$$\frac{d}{dt}(Q_{St} + Q_{Tr}) = \frac{-\mu C_{Tr} W}{2l_{Tr}} \cdot [2KT(\Phi_{mT} - \Phi_{mT0}) + (\Phi_{mT} - \Phi_{mT0})^2] \quad (6a)$$

[6] For example, in applications requiring maximum charge to be transferred along the device (such as digital serial memories and analog delay lines) and if the oxide thickness under the storage gate is 1200 Å, then to operate the device in the complete charge-transfer mode with two-phase drop clock the optimum oxide thickness under the transfer gate is about 3200 Å for $V_m = -15$ V and a substrate doping of 8×10^{14}/cm^3. In other applications such as low level injection CCD imagers it may be more important to maximize the fringing fields under the storage gate. In this case thicker silicon oxides under the storage and transfer gates with a low substrate doping may optimize the performance of the device.

[7] For rise and fall time comparable or larger than the transfer times of interest the same equations given with the push clocks below in (17) and (18) could be used.

[8] A full bucket is the equilibrium surface charge density under the storage gate electrode with its voltage equal to V_m.

[9] The surface-charge and surface-potential profiles are shown in the flip page movie in the issue. The current plots are given in [18].

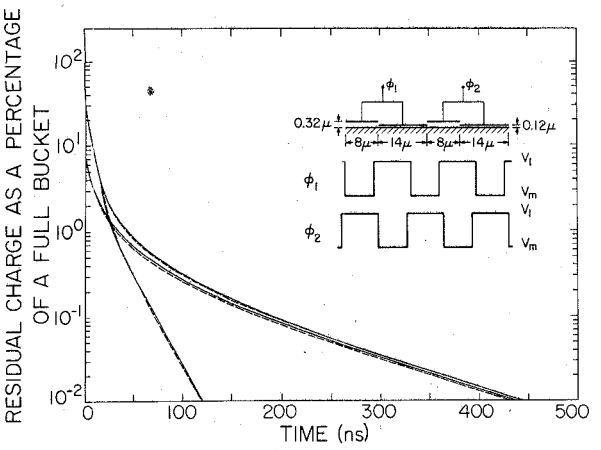


Fig. 3. The residual charge under the storage gate as a percentage of a full bucket for two different initial charges equivalent to about 3 and 1 V versus transfer time. The full line curves are for a substrate doping of 8×10^{14} donors/cm³ and 10^{14} donors/cm³. The dashed line curves are obtained from (7) and (16) according to the lumped-circuit model. $V_m = -15$ V.

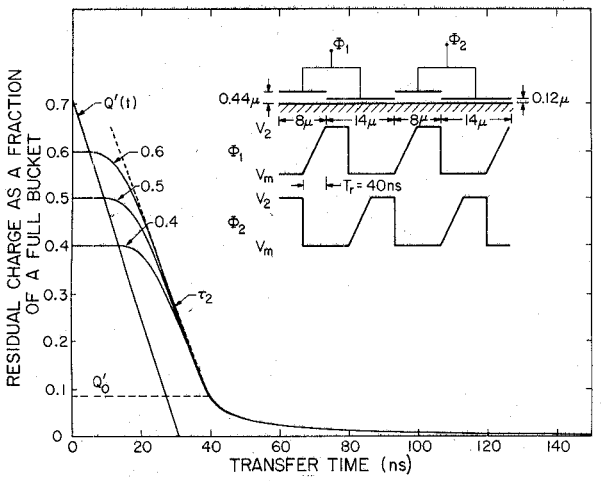


Fig. 4. Residual charge under the storage gate as a fraction of a full bucket for different initial charges versus transfer time, using two-phase push clocks with a rise time $T_r = 40$ ns. The dimensions of the device used are shown at the top of the figure.

$$Q_{st} = Wl_{St}C_{St}(\Phi_{1s} - \Phi_{1s0}), \tag{6b}$$

$$Q_{Tr} = \tfrac{2}{3}Wl_{Tr}C_{Tr}(\Phi_{mT} - \Phi_{mT0}), \tag{6c}$$

$$\Phi_{mT} \cong \Phi_{1s} \qquad \Phi_{mT}' = \Phi_{mT0}, \tag{6d}$$

where Q_{St} and Q_{Tr} are the total charges under the source storage gates and transfer gates. Φ_{1s} and Φ_{1s0} are the surface potential under the source storage gate with and without surface charge when its voltage is equal to V_1. Φ_{mT} and Φ_{mT}' are the surface potential with charge at the beginning and at the end of the transfer gate, respectively, and Φ_{mT0} is the surface potential under the transfer gate without charge when its voltage is equal to V_m. C_{St} and C_{Tr} are the effective oxide and depletion layer capacity under the storage and transfer gates. l_{St} and l_{Tr} are the lengths of the storage and transfer gates, W is the active channel width, and KT the thermal voltage. Since in this stage $(\Phi_{mT} - \Phi_{mT0}) \gg KT$, then for an initial total charge Q_0 the residual charge under the storage gate decreases hyperbolically and is given by

$$Q = \frac{Q_0 + Q'}{1 + \left(\dfrac{t - t_1}{\tau_2}\right)} - Q', \tag{7}$$

where $Q' = Wl_{St}C_{St}(\Phi_{1s0} - \Phi_{mT0})$, t_1 is the time at which the second stage starts, and τ_2 is given by

$$\tau_2 = 2\frac{l_{Tr}l_{St}}{\mu}\frac{C_{St}}{C_{Tr}}\frac{R}{\dfrac{(Q_0 + Q')}{Wl_{St}C_{St}}} \tag{8}$$

where

$$R = 1 + \tfrac{2}{3}\frac{l_{Tr}C_{Tr}}{l_{St}C_{St}}. \tag{9}$$

When the charge under the storage gate decreases to a small value Q_0', the discharge current becomes so small that the electric field in the transitional region between the source storage gate and the next transfer gate can sweep out the carriers fast enough to form an almost perfect sink of charge there.[10] This brings the second stage to an end at a time t_2 given by

$$t_2 = t_1 + \tau_2\frac{Q_0 - Q_0'}{Q_0' + Q'}.$$

For the device parameters given as

$$\begin{aligned} l_{St} &= 13.5\ \mu, \\ C_{St} &= 3.5 \times 10^{-8}\ \text{F/cm}^2, \\ \mu &= 200\ \text{cm}^2/\text{s}\cdot\text{V}, \\ \frac{Q'}{Wl_{St}C_{St}} &= 0.8\ \text{V}, \\ l_{Tr} &= 7\ \mu, \\ C_{Tr} &= 1.45 \times 10^{-8}\ \text{F/cm}^2, \\ \frac{Q_0'}{WlC_{St}} &= 0.48\ \text{V}, \end{aligned} \tag{10}$$

and for a signal charge equivalent to about 3 V we obtain $\tau_2 \cong 6.9$ ns and $t_2 \cong 13.3$ ns. For a signal charge equivalent to about 1 V, we obtain $\tau_2 \cong 14.6$ ns and $t_2 = 5.9$ ns.

3) In the third stage the charge transfer is limited by the transport of charge out of the storage gate with an almost perfect sink at its end. The storage gate can be considered in this stage also as a capacitor discharged through a transfer channel that is the same storage gate. Thus it can be easily shown according to the lumped-

[10] The value of Q_0' at which the perfect sink at the end of the storage gate becomes a good approximation unfortunately cannot be defined precisely. It can be estimated approximately by assuming that the almost perfect sink is formed, when the surface-charge density in the transitional region is about a fifth of its value under the storage gate. Assuming the average surface-potential gradient in the transitional region is $\Delta\Phi/\Delta x$, where $\Delta\Phi$ is the difference in surface potential with no charge under the source storage gate and transfer gate and Δx is the spatial extent of the transitional region (which is equal to about a depletion layer thickness), then Q_0' is given by solving

$$W\mu\frac{\Delta\Phi}{\Delta x}\frac{Q_0'}{Wl_{St}C_{St}}\frac{1}{5} = \frac{(Q_0' + Q')^2}{(Q_0 + Q')}\frac{1}{\tau_2} \rightarrow \frac{(Q_0' + Q')^2}{Q_0'Q'} \cong \frac{1}{5}\cdot\frac{2l_{Tr}}{\Delta x}\cdot\frac{C_{St}}{C_{Tr}}\cdot R.$$

Although the approximate values of Q_0' and t_2 may lead to about 15 percent error in defining the onset of the last two stages, this is a much better approximation than using the perfect sink assumption at the end of the storage gate from the beginning of the charge-transfer process.

circuit model [or by expanding the denominator in (A4–6)] that the residual charge under the storage during the first part of this stage (when $Q(t)/(Wl_{st}C_{st}) > KT$) decreases almost hyperbolically with a time constant τ_3. So,

$$Q(t) = \frac{Q_0'}{1 + \frac{(t - t_2)}{\tau_3}} \qquad t > t_2, \tag{11}$$

$$\tau_3 = \frac{{l_{st}}^2}{\alpha \frac{Q_0'}{C_{st}l_{st}W}\mu} \tag{12}$$

where α is a constant of the order of unity (about 1.2). During this stage the charge is spread over the entire gate even if fringing fields are appreciable.

4) In the last stage of the charge transfer, the self-induced fields become negligible. The residual charge decreases exponentially with a time constant that depends on thermal diffusion and the fringing fields under the storage gate.

For the device we have considered here and for a substrate doping of 8×10^{14} donors/cm^3 and larger, fringing fields under the storage gate are negligible. For $t > t_3$ the residual charge under the storage gate decreases exponentially with the thermal diffusion time constant $\tau_d = {l_{st}}^2/2.5\ D$ [7], where

$$Q(t_3) \sim Wl_{st}C_{st}\ KT \rightarrow t_3 \cong t_2 + \frac{\pi}{2}\tau_d. \tag{13}$$

For the device we have considered and for substrate doping equal to 10^{14} donors/cm^3, solutions of the two-dimensional Poisson equation at the end of the charge transfer show a minimum fringing-field $E_{\min}$ under the storage gate of about 70 V/cm and an average value $\bar{E}$ of about 140 V/cm. The fringing fields considerably enhance the rate of charge transfer. The single-carrier transit time across the storage gate t_{tr} due to fringing fields is given by

$$t_{tr} = \int_{\substack{\text{over storage}\\ \text{gate length}}} \frac{dy}{\mu E(y)} = \frac{l_{st}}{\mu \bar{E}} = \frac{{l_{st}}^2}{\mu \Delta\Phi}, \tag{14}$$

where $\bar{E}$ is the average fringing field under the storage gate, $\Delta\Phi$ is equal to $\bar{E}l_{st}$ and is related to the voltage drop across the storage gate due to fringing fields.

Under the influence of the fringing fields, the charge profile under the storage gate starts to drift after a time $t_3 \simeq t_2 + t_{tr}$ for about one single-carrier transit time and then becomes stationary at a position that depends on the minimum fringing-field $E_{\min}$. The residual charge then decreases exponentially with a final decay time constant given approximately by

$$\frac{1}{\tau_f} \cong 4\left(\frac{\pi^2 D}{4{l_{st}}^2}\right) + \frac{(\mu E_{\min})^2}{4D}. \tag{15}$$

The factor 4 in the second term is due to the large fields at the edges of the gate. For negligible fringing fields this factor takes a value of unity. The exponential decay is due to the diffusion at the tail end of the residual charge packet under the storage gate irrespective of the fringing-field profile. Fringing fields alone, without diffusion and self-induced fields, will sweep out the residual charge under the storage gate in a single carrier transit time. A more detailed discussion of the effect of fringing fields on the charge transfer is given in [9] and [21].

The transition between the hyperbolic regime of the third stage and the exponential regime of the last stage of the charge is rather broad and is best described by (A4–8) in Appendix IV.

$$\frac{Q_{st}}{Q_0'} \approx \frac{\exp\left(-(t - t_2)/\tau_f\right)}{1 + \frac{Q_0'}{\frac{2}{3}C_{st}l_{st}W}\cdot\frac{1}{2KT}\cdot\frac{\tau_f}{\tau_d}\left[1 - \exp\left(-(t - t_2)/\tau_f\right)\right]}. \tag{16}$$

The dashed lines[11] in Fig. 3 are obtained from (7) and (16) with the device parameters given in (10).

Push Clocks: With push clocks the charge is stored under a gate held at V_m that is the largest clock voltage the MOS structure can tolerate. The charge is transferred to a nearby gate also at V_m by raising the potential of the gate where the charge has been residing and thus pushing the charge to the next gate [26].

For optimum operation of the device with two-phase push clock in the complete charge-transfer mode, the oxide thickness under the storage and transfer gates should be properly chosen.[12]

We have simulated numerically the charge-transfer characteristics for several devices with various clocking waveforms. In Figs. 4 and 5 we have plotted the residual charges under the source storage gate versus transfer time. The clock voltages and rise time as well as the oxide thickness under the transfer gates of the device are shown for each case at the top of the figures. Zero time coincides with the instant the clock voltage starts to increase to push the charge and starts the transfer process.

From the plots of the transient currents at the end of the transfer gate and the residual charges versus time and the surface charge and surface-potential profiles under the gates[13] one can identify several distinct stages of the charge transfer.

1) In the first stage, the surface potential under the storage gate containing charge increases as the storage gate voltage is increasing, until it becomes equal or less

[11] The good fitting in Fig. 3 to the numerical solution is partly because the precise values of Q_0' and t_2 could be obtained from the time evolution of the numerically calculated surface-potential profiles under the gates.

[12] Note that in the overlapping gate two phase structure, the asymmetry is obtained by the step in the oxide under the two electrodes connected to the same phase, therefore a larger signal charge could be stored under the storage gate with push clock than with drop clocks. Also the maximum signal charge increases as the oxide thickness increases. The limits on the oxide thickness under the transfer gates are imposed by the following two factors. First, as the oxide thickness under the transfer gates increases the maximum current that can be transferred across it, which is the saturation current of a similar MOS transistor, decreases. Thus the rate of charge transfer during the first stages of the transfer process decreases. Second, if the oxide is too thick the regions under the transfer gates will go into majority carrier accumulation, when its phase voltage is at the resting potential V_2. Thus the majority carriers fill the traps and recombination centers at the interface and may recombine with the signal minority carriers during the charge transfer. The charge loss in this case is not as severe as the case when the regions under the storage gates are driven into accumulation [27], because the signal charge does not spend as much time under the transfer gates as it spends under the storage gate. This phenomenon does not impose severe limitations, but it is preferable to keep the regions under the transfer gates always depleted to avoid the second order effects of charge loss especially for long registers.

[13] The surface-charge and surface-potential profiles under the gates for the case shown in Fig. 4 are illustrated in the flip page movie in this issue. The current plots are given in [18].

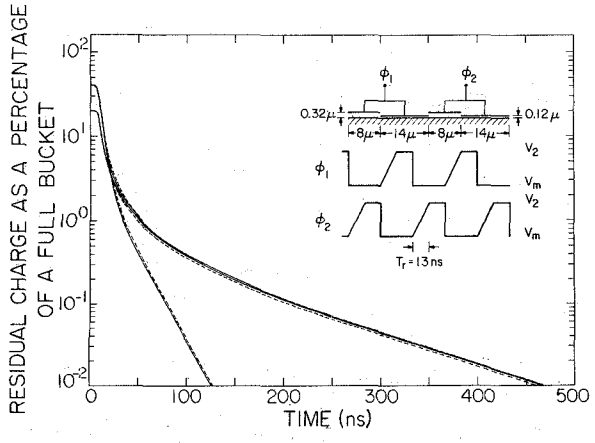


Fig. 5. The residual charge under the storage gate as a percentage of a full bucket for two different initial charges 0.2 and 0.42 of a full bucket for a device with 3200 Å under the transfer gate. The full line curves are for a substrate doping of 8×10^{14} donors/cm^3, and 10^{14} donors/cm^3. The dashed line curves are obtained from (16) and (18) according to the lumped-circuit model. $V_m = -15$ V, $T_r = 13$ ns.

than the surface potential under the next transfer gate by KT. Then the charge initially confined under the storage gate spreads to charge up the next transfer gate. The time interval of the first part of this stage depends on the amount of initial charge and the clock rise time as given in (19).

2) The second stage of the charge transfer is limited by the transport of charge cross the transfer gate to the next storage gate. The transfer gate acts as an MOS transistor at pinchoff, and the storage gate as its source and drain. For maximum rate of discharge in this stage, the gate voltage should be rising with a rate that keeps the surface potential under the storage gate at a value that does not exceed $2\Phi_F$ to avoid injection of the signal charge into the substrate where Φ_F is the Fermi potential of the substrate. Since the surface potential under the gate varies almost linearly with the stored charge and the gate voltage, the maximum rate of charge transfer can be achieved by clocking waveforms with ramps of a slope that matches the saturation current of the transfer gate.

According to the lumped-circuit model discussed in Appendix IV the decay of the residual charge under the storage gate in this stage can be described by the following equations.

$$\frac{d}{dt}(Q_{st} + Q_{Tr}) = -\frac{\mu C_{Tr} W}{2l_{Tr}} \cdot [2KT(\Phi_{mT} - \Phi_{mT0}) + (\Phi_{mT} - \Phi_{mT0})^2] \quad (17a)$$

$$Q_{st} = W l_{St} C_{St}(\Phi_s - \Phi_{s0}) \quad (17b)$$

$$Q_{Tr} = \tfrac{2}{3} W l_{Tr} C_{Tr}(\Phi_{mT} - \Phi_{mT0}) \quad (17c)$$

$$\Phi_{mT} \cong \Phi_s; \qquad \Phi_{mT}' \cong \Phi_{mT0} \quad (17d)$$

$$\Phi_{s0} = B_{1s} V + B_{2s} \quad \text{and} \quad \Phi_{mT0} = B_{1T} V_m + B_{2T} \quad (17e)$$

where V and V_m are the voltages of the first and second phases, driving the source storage gate and transfer gate, respectively. B_{1s}, B_{2s}, B_{1T}, and B_{2T} are constants chosen to give the best linear fit to the relation of the surface potential under the storage and transfer gates to the voltage applied to them. The rest of the notation is similar to that in (6). For clocking waveforms with ramps or with sufficiently smooth driving function[14] and for an initial charge Q_0 the residual charge under the storage gate is given by

$$Q = Q'(t) + Q'' \tanh((t - t_1)/\tau_2) \quad (18a)$$

where

$$Q'(t) = W l_{St} C_{St}(\Phi_{mT0} - \Phi_{s0}) \quad (18b)$$

$$Q'' = W l_{St} C_{St} \sqrt{\frac{2 l_{Tr} l_{St}}{\mu} \frac{C_{St}}{C_{Tr}} \frac{d}{dt}(\Phi_{s0} - \Phi_{mT0})} \quad (18c)$$

and

$$\tau_2 = R \sqrt{\frac{2 l_{Tr} l_{St}}{\mu} \frac{C_{St}}{C_{Tr}} \frac{1}{\frac{d}{dt}(\Phi_{s0} - \Phi_{mT0})}} \quad (18d)$$

$$R = 1 + \tfrac{2}{3} \frac{l_{Tr} C_{Tr}}{l_{St} C_{St}}. \quad (18e)$$

t_1 is the time at which the discharge current I starts to flow. The value of $Q'(t)$ is the minimum initial charge under the source storage gate that causes the discharge current I to start at time t. Hence, for a given initial charge Q_0, t_1 is given by

$$Q'(t_1) = Q_0. \quad (19)$$

It follows directly from (18) that for a ramp clocking waveform the minimum rise time $Tr|_{\min}$ of the clocking voltage to prevent injection of the signal charge in the substrate is given by

$$Tr\,|_{\min} = \frac{2 l_{Tr} l_{St}}{\mu} \frac{C_{St}}{C_{Tr}} \frac{B_{1s}(V_2 - V_m)}{(2\Phi_F - \Phi_{mA0})^2}, \quad (20)$$

where V_2 and V_m are the resting and minimum voltages of the clock. For $(t - t_1) > \tau_2$ the residual charge under the storage gate decreases according to the waveform of $V(t)$.

The parameters of the device used in the numerical simulation are given here.

$$l_{St} = 13.5\ \mu, \qquad l_{Tr} = 7\ \mu,$$
$$C_{St} = 3.14 \times 10^{-8}\ \text{F/cm}^2, \qquad B_{1s} = 0.9162,$$
$$V_m = -15\ \text{V}, \qquad \mu = 200\ \text{cm}^2/\text{V·s}. \quad (21)$$

If the oxide thickness under the transfer gate is 3200 Å and $V_2 = -6$ V and $T_r = 13$ ns, then $C_{Tr} = 1.45 \times 10^{-8}$F/cm^2, $T_{r|\min} \cong 5.5$ ns, and $\tau_2 \cong 6.5$ ns. If the oxide thickness under the transfer gate is 4400 Å and $V_2 = -3$ V and $T_r = 40$ ns, then $C_{Tr} = 1.32 \times 10^{-8}$F/cm^2, $T_{r|\min} \cong 21$ ns, and $\tau_2 = 11.5$ ns.

3) In the third stage the clock voltages are constant and the charge transfer is limited by the transport of charge out of the storage gate with an almost perfect sink

[14] For arbitrarily smooth waveforms solution of (17) can be easily obtained analytically using Ricatti's substitution and the Wentzel–Kramer–Brillouin–Jeffreys (WKBJ) method [28]. The final solutions are similar to the results reported by Thornber [29] for the MOS bucket brigade. For sinusoidal drive functions the solutions can be written in terms of Mathieu functions. We mean by sufficiently smooth drive function that the time dependence of

$$\frac{2 l_{Tr} l_{St}}{\mu} \frac{C_{St}}{C_{Tr}} \frac{d}{dt}(\Phi_{s0} - \Phi_{mT0})$$

is much smaller than that of $(\Phi_{mT} - \Phi_{mT0})^2$.

at its end. The storage gate in this stage is discharged through itself as in the case of the drop clock. The residual charge under the storage gate $Q(t)$ decreases during the first part of this stage hyperbolically with a time constant τ_3.

$$Q(t) = \frac{Q_0'}{1 + \dfrac{t - t_2}{\tau_3}} \qquad t > t_2, \tag{22}$$

where

$$\tau_3 = \frac{{l_{St}}^2}{\alpha \dfrac{Q_0'}{C_{St} l_{St} W} \mu}$$

and Q_0' is the total charge under the source storage gate when the perfect sink at its end is formed at time t_2. t_2 is approximately[15] equal to T_r and Q_0' is obtained from (18) with $t = t_2$.

4) In the last stage the residual charge decreases exponentially with a time constant that depends on thermal diffusion and fringing fields under the storage gate as discussed previously in (13)–(16).

Incomplete Charge-Transfer Mode

In the incomplete (or residual) charge-transfer mode, a bias charge is deliberately retained under the storage gates at each transfer. This can be achieved by controlling the resting surface potential under the storage gate relative to that under the next transfer gate at the end of the charge-transfer process [11], [30]. In the two-phase clocking scheme, for a given substrate doping and minimum voltage V_m the oxide thickness under the storage and transfer gates should also be properly chosen for optimum device operation in this mode.

We have simulated numerically the charge transfer for the device shown at the top of Fig. 6 clocked by a two-phase push clock in the incomplete charge-transfer mode with a bias charge equivalent to about 1 V. We have plotted in Fig. 6 the residual charge under the source storage gate as a fraction of a full bucket versus transfer time for two different initial charges 0.6 and 0.4 of a full bucket. From the plots of the currents at the ends of the gates and the residual charges versus time and the surface-charge and surface-potential profiles under the gates one can identify distinct stages of the charge transfer. The first two stages are similar to the first two stages of the two-phase push clock case described before. The third stage starts when the clock voltage stops at time $t_2 = T_r$ with a residual charge under the source storage gate equal to Q_0'.

The charge transfer in the first part of this stage

$$\left(\frac{Q(t) - Q'}{W l_{St} C_{St}} > 2KT\right)$$

is similar to the charge transfer in the second stage of the two-phase drop clock discussed previously in (7)–(9). The residual charge is thus given by

[15] Actually the perfect sink may be formed before or after the clock voltage stops changing. The value of t_2 unfortunately cannot be evaluated precisely and this may lead to about 15 percent error in locating the exponential tail of the last stage of the charge transfer. If $t_2 > T_r$, then after the clock voltage stops the residual charge under the storage gate decreases hyperbolically with a time constant τ_3 as given by (7)–(9). If $t_2 < T_r$ then the perfect sink is formed before the clock voltage stops. In Fig. 5 the good fitting to the numerical solution is because the precise values of t_2 could be obtained from the numerically calculated surface-charge profiles under the gates.

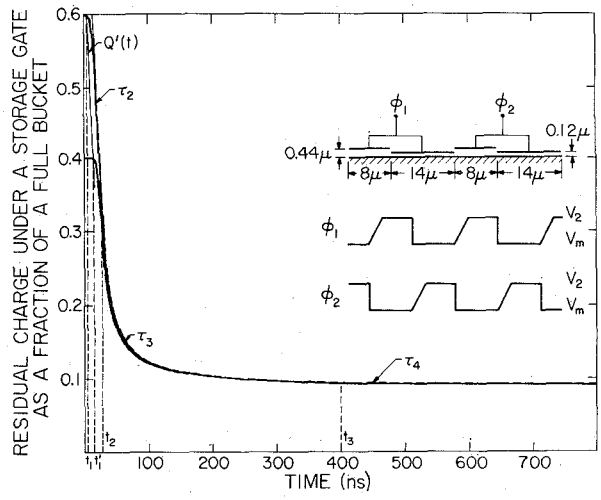


Fig. 6. The residual charge as a fraction of a full bucket for two different initial charge 0.6 and 0.4 of a full bucket versus transfer time. The device is operated with two-phase push clock in the incomplete charge-transfer mode. The dimensions of the device used are shown at the top of the figure. The dashed line curves are obtained from (18), (23), and (27) according to the lumped-circuit model.

$$Q(t) = \frac{Q_0' - Q'}{1 + \dfrac{(t - t_2)}{\tau_3}} + Q', \tag{23a}$$

where

$$\tau_3 = \frac{2 l_{St} l_{Tr}}{\mu} \frac{C_{St}}{C_{Tr}} \frac{R}{\dfrac{Q_0' - Q'}{W C_{St} l_{St}}}. \tag{23b}$$

Q' is the bias charge and is equal to $W l_{St} C_{St} (\Phi_{mT0} - \Phi_{1s0})$. This stage ends at time t_3 when

$$Q(t_3) - Q' \simeq W C_{St} l_{St} \cdot 2KT \rightarrow t_3 = t_2 + \frac{l_{St} l_{Tr}}{D} \frac{C_{St}}{C_{Tr}} \cdot R. \tag{24}$$

In the last stage of the charge transfer, the surface potential under the storage gate drops below that under the transfer gate. However, the discharge current still continues to flow due to thermal emission of the carriers under the storage gate over the potential barrier. The mobile charge under the transfer gate also becomes so small that thermal diffusion becomes dominant. Fringing fields under the transfer gate are usually small because the surface potential under the transfer gate and the preceding storage gate are almost equal. The residual charge under the storage gate in this stage decreases logarithmically with time. Using the lumped circuit described in Appendix IV the charge transfer in the incomplete charge-transfer mode is described by the following equations.

$$\frac{d}{dt}(Q_{st} + Q_{Tr}) = -\frac{\mu C_{Tr} W}{2 l_{Tr}} \cdot [2KT(\Phi_{mT} - \Phi_{mT0}) + (\Phi_{mT} - \Phi_{mT0})^2] \tag{25a}$$

$$Q_{st} = W l_{St} C_{St} (\Phi_{1s} - \Phi_{1s0}) \tag{25b}$$

$$Q_{Tr} = \tfrac{2}{3} W l_{Tr} C_{Tr} (\Phi_{mT} - \Phi_{mT0}) \frac{[(\Phi_{mT} - \Phi_{mT0}) + \frac{3}{2}KT]}{[(\Phi_{mT} - \Phi_{mT0}) + 2KT]} \tag{25c}$$

$$C_{Tr}(\Phi_{mT} - \Phi_{mT0}) = C_{St}(\Phi_{1s} - \Phi_{1s0}) \cdot \exp\left(-(\Phi_{mT} - \Phi_{1s})/KT\right); \ \Phi_{mT}' = \Phi_{mT0} \tag{25d}$$

$$\left[1 + \frac{KT}{\Phi_{mT} - \Phi_{mT0}}\right] \cdot \frac{d}{dt}(\Phi_{mT} - \Phi_{mT0}) = \left[1 + \frac{KT}{\Phi_{1s} - \Phi_{1s0}}\right] \cdot \frac{d}{dt}(\Phi_{1s} - \Phi_{1s0}) + \frac{d}{dt}(\Phi_{1s0} - \Phi_{mT0}). \quad (25e)$$

Assuming a sufficiently large bias charge ($Q' \gg KT\,Wl_{St}C_{St}$) and taking $(\Phi_{mT} + KT)(\Phi_{mT} + 3KT) \approx (\Phi_m + 2KT)^2$, then (25) is reduced to

$$-\frac{\mu C_{Tr} W}{2l_{Tr}}[(\Phi_{mT} - \Phi_{mT0})^2 + 2KT(\Phi_{mT} - \Phi_{mT0})] = \left[Wl_{St}C_{St}\left(1 + \frac{KT}{\Phi_{mT} - \Phi_{mT0}}\right) + \tfrac{2}{3}Wl_{Tr}C_{Tr}\right] \cdot \frac{d}{dt}(\Phi_{mT} - \Phi_{mT0}). \quad (26)$$

For $(\Phi_{mT} - \Phi_{mT0}) < KT$ the residual charge under the source storage gate is given by[16]

$$Q(t) = Q' - KTWl_{St}C_{St} \ln [1 + (t - t_3)/\tau_4] \quad (27a)$$

where

$$\tau_4 = \frac{l_{Tr}l_{St}}{2D}\frac{C_{St}}{C_{Tr}}. \quad (27b)$$

If $t > t_4 = t_3 + \tau_4 \exp(Q'/Wl_{St}C_{St}KT)$, (25) reduces to

$$Q(t) \sim C_{St}KTWl_{St} \exp(-(t - t_4)/\tau_5), \quad (28a)$$

where

$$\tau_5 = \frac{l_{Tr}l_{St}}{D} \exp((\Phi_{mT0} - \Phi_{1s0})/KT). \quad (28b)$$

However for a bias charge equivalent to 1 V, t_4 and τ_5 are larger than the interface storage time [31] of the best thermally grown oxide and hence that stage will never be reached practically. If fringing fields under the transfer gate are appreciable for a closer spacing device or a lower substrate doping, then the previous relations still hold except D/l_{Tr} is replaced by $(\mu\bar{E} + D/l_{Tr})$ where $\bar{E}$ is the average fringing field under the transfer gate.

When a static two-phase drop clock is used to operate the device in the incomplete charge transfer, the two first stages of the charge transfer are similar to the two first stages of the static drop clock in the complete charge-transfer mode. However in the last stage, the residual charge in the incomplete charge-transfer mode decreases logarithmically according to (27).

[16] The residual charge under the source storage gate during the last two stages (after the clock voltage stop) given by (23) and (27) can be approximately described by one equation if we assume that

$$\frac{[(Wl_{St}C_{St} + \tfrac{2}{3}Wl_{Tr}C_{Tr})(\Phi_{mT} - \Phi_{mT0}) + Wl_{St}C_{St}KT]}{[(\Phi_{mT} - \Phi_{mT0}) + 2kT]} = Wl_{St}C_{St}.$$

Then (27) can be solved to give

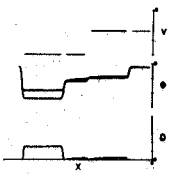
$$Q(t) \cong Q' + \frac{Q_0' - Q'}{1 + \dfrac{(t - t_2)}{\tau}} - KTWl_{St}C_{St} \ln\left(1 + \frac{(t - t_2)}{\tau}\right)$$

where

$$\tau = \frac{2l_{St}l_{Tr}}{\mu}\frac{C_{St}}{C_{Tr}}\frac{1}{\dfrac{Q_0' - Q'}{Wl_{St}C_{St}}}.$$

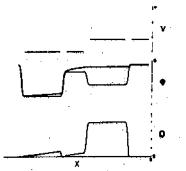
IV. Four-Phase Clocking Scheme

In the overlapped gates CCD's, four-phases may be used to control the storage and transfer of charge along the interface. Since each gate electrode is driven by a separate phase, more flexibility in operating the device is expected. With four-clocking phases the polysilicon electrodes can be used to store the signal charge and the aluminum electrodes to control the transfer and storage process, or both the polysilicon and aluminum gates can be used as storage sites. The latter method requires four transfers/bit and the aluminum electrode should have the same areas as the polysilicon electrodes, but the former method requires two transfers/bit and the aluminum electrodes can have a smaller area. We will consider the first method as it requires less area/bit and results in less signal degradation due to incomplete free charge transfer.



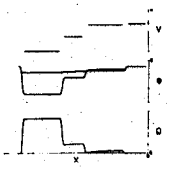
Complete Charge-Transfer Mode

Drop Clock: With the four-phase drop clock, the minimum and resting voltages (V_m' and V_2') of the clock phases driving the transfer gates can be independently controlled whatever is the oxide thickness under the transfer electrodes for operation in the complete charge-transfer mode. The stages of the charge-transfer process are similar to the two-phase drop clocks [17], [26]. So increasing the complexity of the clock from two-phases to four-phases with drop clock does not improve the performance of the device.



Push Clock: Push clocks take full advantage of the more flexible control of the storage and transfer of charge with the four-phases of the clock. At the top of Fig. 7, we show the device dimensions and the clocking waveforms we have used in our computer simulation of the four-phase push clock.

Since with four-clocking phases the preceding transfer gate can be turned off by the resting voltage V_2', the maximum signal charge that can be stored under the storage gate with its voltage equal to V_m can be almost a full bucket. In the two-phase clocking scheme, each set of transfer and storage gate is driven by the same phase of the clock so the preceding transfer gate is turned on when the storage gate is turned on. Hence, the maximum charge that can be stored with four-phase push clock is larger than with two-phase clock for the same voltage amplitude. To transfer the charge for example, from under the first storage gate to the second one, ϕ_{2A} and ϕ_{2B} drops to V_m to turn on heavily the second transfer and storage gate. Then ϕ_{1B} increases to push the charge from under the first storage gate to the adjacent gates. Then ϕ_{2A} increases to push the charge to the next storage gate. As ϕ_{2A} reaches the resting voltage V_2', the charge transfer ends and some of the residual charge under the transfer gate spills back to the preceding storage gate. The rate of rise of ϕ_{2A} should be sufficiently slow so that the amount of charge under the transfer gate that spills back to the preceding storage gate is small. Therefore, the rise time T_r of the transfer gate clock should increase with the increase of the clock bit time.



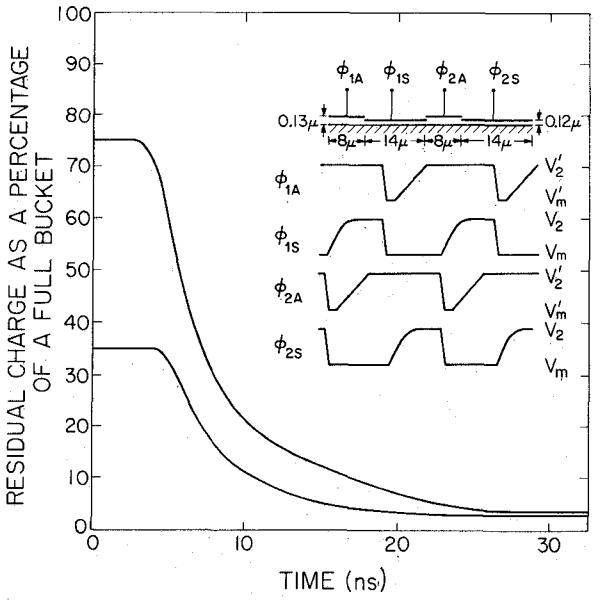


Fig. 7. The residual charge under the storage gate for two different initial charges 0.75 and 0.35 of a full bucket versus transfer time with the four-phase push clock. The dimensions of the device and the clocking waveforms used are shown at the top of the figure.

In Fig. 7 we have plotted the residual charge under the storage gate for two different initial charges 0.75 and 0.35 of a full bucket. With the four-phase push clock, more charge can be stored and much faster rates of charge transfer in the first stages of the transfer process can be achieved since the transfer gates can be controlled independently. However, in the last stages of the charge-transfer process, the residual charge decreases exponentially with a time constant that depends on thermal diffusion and fringing fields as with the two-phase clocks.

Incomplete Charge-Transfer Mode

In the incomplete charge-transfer mode, a bias charge is left under the storage gate at each transfer. Whether push or drop four-phase clocks are used, the first stages of the charge transfer will be similar to those in the complete charge-transfer mode. But in the last stage of the charge transfer, the residual charge under the storage gate does not decrease exponentially as in the complete charge-transfer mode, but it decreases logarithmically with a much slower rate.

V. Discussion and Conclusion

We have developed a detailed numerical simulation of the transport dynamics in terms of charge motion due to thermal diffusion, self-induced fields, and fringing fields under all the relevant electrodes and interelectrodes regions of CCD's. This numerical simulation is a simple mathematical model that can be used to study the free charge-transfer characteristics of different device structures with various clocking schemes and waveforms. We have also presented the charge-transfer characteristics of overlapping gate CCD's clocked with two- and four-phase clocks and various waveforms.

The charge transfer with three-phase and single-phase clocking schemes can be readily understood from the results of the numerical simulation of the charge transfer with two- and four-phase clocking schemes. The charge transfer with a single-phase clocking scheme can be easily deduced from the charge transfer with the push and drop two-phase clocks. The charge transfer with dynamic three-phase push clock also follows from the charge transfer with the four-phase push clock [17], [18].

We have shown that the charge transfer in the overlapping gate structure divides naturally into several distinct stages. In the first stages, the storage gates are like capacitors charged and discharged by the transfer gates that limit the transfer rate. The overlapping transfer gate shields out the repulsive forces of the surface charge in transit and enhances the rate of charge transfer. The nonlinearity due to the self-induced fields is dominant in these stages and the charge transfer depends on the clocking waveforms. In the two-phase clocking scheme the transfer gates are like MOS transistors at pinchoff, and the storage gates are the sources and the drains. In these stages the transferred charge increases according to the portion of the clock voltage waveform that pushes the charge from one storage site to another for the push clocks, or according to the portion of the clock voltage waveform that creates the deeper potential well for the drop clocks.

The last stages of the charge-transfer process depend on whether the device is operated in the complete charge-transfer mode or in the incomplete charge-transfer mode. During the last stages of the complete charge-transfer mode the rate of charge transfer in the overlapping gate structure depends on how fast the storage gates can be discharged. The transfer gates in this structure are usually shorter and have larger fringing fields, and the charge transfer across the transfer gates is much faster than the charge transfer out of the storage gate. In the last stage, the residual charge under the storage gate decreases exponentially with a time constant that depends on fringing fields and thermal diffusion. For strong fringing fields, the final decay time constant τ_f is a fraction of the single-carrier transit time across the storage gate. In this case the exponential decay is due to the diffusion at the tail end of the residual charge packet under the storage gate. In the incomplete charge-transfer mode, the charge transfer is very similar to the charge transfer in the MOS bucket brigade [19]. In this case, the charge transfer in the last stage is dependent on the transfer gate length. The residual charge under the storage gate decreases logarithmically, due to the thermally emitted carriers from the residual charge that diffuses across the transfer gate to the next storage gate.

The time constants of all stages of the charge transfer are proportional to the product of the storage gate and transfer gate lengths or the storage gate length squared, and the inverse of the surface mobility. In the first stages, the time constants are proportional to the inverse of the portion of the clock voltage used to store the signal charge. In the last stages the time constants are proportional to the inverse of the thermal voltage or the voltage drop across the gates due to fringing fields.

We have shown also that the charge-transfer characteristics calculated from a lumped-circuit model of the overlapping gate CCD's agree with the results of the numerical simulation. According to this model, the charge-transfer dynamics could be described by the charging and discharging of lumped capacitors through lumped-transfer channels. This is possible because the redistribution times of the surface charges under the CCD gates are orders of magnitude smaller than the transfer times and therefore the surface charge profiles under the gates reach steady state. The lumped-circuit model can be used to derive the charge transfer characteristics for other device structures and dimensions with various clocking waveforms and voltages, thus providing practical CCD and circuit design tools.

The signal degradation due to incomplete free charge transfer can be calculated from the charge transfer characteristics obtained from the numerical simulation or the lumped-circuit model of the free charge-transfer process. These calculations [17], [18] show that the signal degradation of the incomplete free charge is due to an intrinsic transfer rate and due to the modulation of the device parameters by the signal charge being transferred. The intrinsic transfer rate is due to the finite carrier mobility and finite transfer time. The modulation effects are due to the dependence of the effective lengths of the gates, the effective capacitances per unit area and fringing fields under the storage and transfer gates on the signal charge being transferred.

Calculations of the signal degradation due to incomplete charge transfer (plotted in Fig. 8) show that the performance of the overlapping gate CCD is better than the MOS bucket brigade. At very high clock frequency the signal degradation due to incomplete free charge transfer in the MOS bucket brigade is almost the same as in the overlapping gate CCD. But at moderate and low clock frequency the signal degradation in the MOS bucket brigade is larger than in the overlapping gate CCD. The MOS bucket brigade always operate in the incomplete charge-transfer mode; the p islands are storage buckets with undefined bottoms that always contain residual charge. So the residual charge decreases logarithmically with time and the signal degradation tends to a constant value at low clock frequency due to transfer gate length and barrier height modulation.[17] But the overlapping gate CCD's can be operated in the complete charge-transfer mode. So the residual charge decreases exponentially and the signal degradation due to incomplete free charge transfer (intrinsic transfer rate and device parameters modulation) also decreases exponentially with time. The signal degradation due to trapping in the interface states, which is the dominant effect in the overlapping gate CCD at low clock frequency [15], is also less than the signal degradation in the MOS bucket brigade [19] at low clock frequency.

Calculations of the signal degradation due to incomplete charge transfer (plotted in Fig. 8) also show that the signal degradation with push clocks is less than with drop clocks. This is because with push clocks the residual charges after each transfer are more independent of the initial charge than with drop clocks. The differences in the charge-transfer characteristics and the mobile charge profiles under the CCD gates and the interaction of the charges with the interface states depending on whether a large or small charge is being transferred are minimized with push clocks [26].

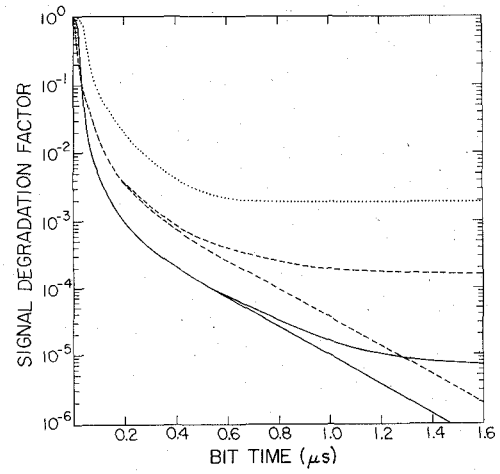
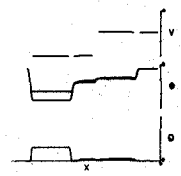
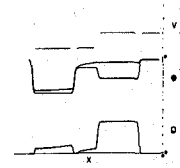
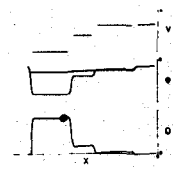


Fig. 8. Signal degradation factor $\epsilon(\epsilon = \Delta Q_r/\Delta Q_i$, where ΔQ_r is the change in the residual charge after each transfer due to a change in the initial charge ΔQ_i) versus bit time. The dotted curve is the signal degradation factor due to incomplete free charge transfer (intrinsic transfer rate and device parameters modulation) for the case described in Fig. 6 where the device is operated with a two-phase push clock in the incomplete charge transfer mode (similar to the MOS bucket brigade). The dashed and full line curves are the signal degradation factors for the cases described in Figs. 3 and 5, where the device is operated with a two-phase drop and push clock in the complete charge transfer mode, respectively. The lower dashed and full line curves represent the signal degradation factor due to incomplete free charge transfer (intrinsic transfer rate and device parameter modulation). The upper dashed and full line curves represent the signal degradation factor of the incomplete free charge transfer and incomplete charge transfer due to trapping in the interface states.

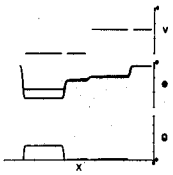




The plots of the residual charge due to incomplete free charge transfer versus the initial charge with any clocking waveform show saturation characteristics as shown in Fig. 9 due to the strong nonlinearity inherent in the transport dynamics. The plots of the net residual charge due to trapping in interface states versus the initial charge show also the same saturation shape. For larger charge, the residual charge tends to be less dependent on the initial charge. This saturation characteristic indicates that the signal degradation due to incomplete free charge and trapping in interface states can be considerably reduced by using a circulating background charge or fat zero to represent the zero signal. Also the saturation characteristic indicates that for digital signal applications due to incomplete charge transfer the optimum size of the fat zero which results in maximum signal output increases by increasing the clock frequency and the number of stages in the charge-coupled shift register [17], [18] and is independent of the size of the 1-bit charge.



[17] Barrier height modulation results in a modulation of the residual charge in the storage sites.



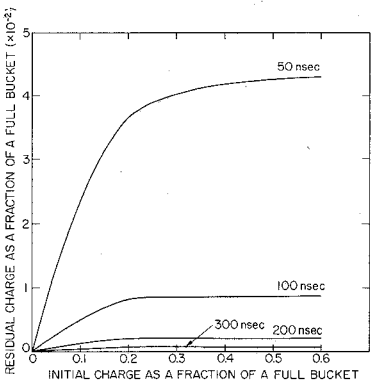
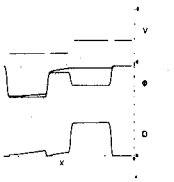
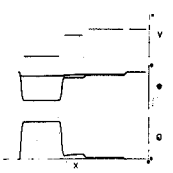


Fig. 9. Residual charge versus initial charge at different transfer times for two-phase push clock.





Appendix I
Green's Function Solution of the Potential in a MIS Structure

Consider a MIS structure as shown in Fig. 10. The insulator-semiconductor interface, and the insulator-metal interface are parallel to the y–z planes. It is desired to estimate the surface potential and the surface-potential gradient at the semiconductor-insulator interface, for an arbitrary surface-charge density profile $q(y)$ and a voltage V_G on the metal electrode. Although the Poisson equation for this problem is nonlinear in the semiconductor region, we may still solve it as a linear equation using the depletion approximation. First, let us calculate the potential and electric field at any point (x, y) in the semiconductor region due to a linear charge of unit strength, i.e., 1 C/cm, at a point (x', y') parallel to the z-axis. The semiconductor region, in this case, is treated as a dielectric of permittivity ϵ_1. The resulting potential function $G(x, y, x', y')$ is the Green's function solution of the two-dimensional Poisson equation of the structure. Assuming the metal plane is at ground potential, the desired potential function can be calculated by the method of images. Since the boundary conditions at both the insulator-semiconductor interface and insulator-metal interface should be satisfied, an infinite series of image line charges are required to calculate the potential function in each region. It can be shown that the Green's function in the semiconductor region is given [32] by

$$G(x, y, x', y') = \frac{-1}{4\pi\epsilon_1}\left\{\frac{\epsilon_1 - \epsilon_2}{\epsilon_1 + \epsilon_2}\ln\left[(y - y')^2 + (x + x')^2\right] + \ln\left[(y - y')^2 + (x - x')^2\right] - \frac{4\epsilon_1\epsilon_2}{(\epsilon_1 + \epsilon_2)^2}\sum_{m=1}^{\infty}\left(\frac{\epsilon_1 - \epsilon_2}{\epsilon_1 + \epsilon_2}\right)^{m-1} \cdot \ln\left[(y - y')^2 + (x + x' + 2md_0)^2\right]\right\} \quad \text{(A1-1)}$$

where d_0 is the insulator thickness.

If the point (x, y) lies at the semiconductor-insulator interface, then substituting in (A1-1) we get

$$G(0, y, x', y') = \left\{\frac{-1}{2\pi(\epsilon_1 + \epsilon_2)}\ln\left[(y - y')^2 + x'^2\right] - \frac{\epsilon_2}{\epsilon_1 + \epsilon_2}\sum_{m=1}^{\infty}\left(\frac{\epsilon_1 - \epsilon_2}{\epsilon_1 + \epsilon_2}\right)^{m-1} \cdot \ln\left[(y - y')^2 + (x' + 2md_0)^2\right]\right\}. \quad \text{(A1-2)}$$

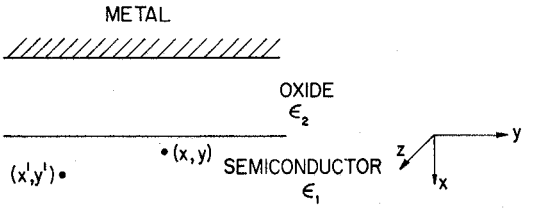


Fig. 10. Metal-insulator semiconductor system. The potential at any point in the semiconductor (x, y) due to a line charge parallel to the z axis at (x', y') is calculated using the method of images.

The Green's function of the surface-potential gradient along the semiconductor-insulator interface is given by

$$\frac{\partial}{\partial y}G(0, y, x', y') = \frac{-1}{\pi(\epsilon_1 + \epsilon_2)}\left\{\frac{y - y'}{(y - y')^2 + x'^2} - \frac{2\epsilon_2}{\epsilon_1 + \epsilon_2} \cdot \sum_{m=1}^{\infty}\left(\frac{\epsilon_1 - \epsilon_2}{\epsilon_1 + \epsilon_2}\right)^{m-1}\frac{(y - y')}{(y - y')^2 + (x' + 2md_0)^2}\right\}. \quad \text{(A1-3)}$$

The surface potential for a surface-charge density profile $q(y')$ and a gate voltage V_G is given by (neglecting the fixed insulator-semiconductor interface charge q_{ss}, and the difference in the metal and semiconductor work functions)

$$\Phi_s(y) = \Phi(0, y) = V_G + \int_{-\infty}^{+\infty} G(0, y, 0, y')q(y')\,dy' + \int_{-\infty}^{+\infty} dy \int_0^{X_D(y')} dx' G(0, y, x', y')eN_D \quad \text{(A1-4)}$$

where N_D is the donor concentration for n-semiconductor. $X_D(y)$ is the depletion layer thickness defined by the implicit relation

$$\Phi(x_D, y) = V_G + \int_{-\infty}^{+\infty} G(x_D, y, 0, y')q(y')\,dy' + \int_{-\infty}^{+\infty} dy' \int_0^{X_D(y')} G(x_D, y, x', y')eN_D\,dy' = 0. \quad \text{(A1-5)}$$

It can be shown from (A1-1) and (A1-2) that

$$G(x, y, x', y') = G(x, x', y - y') \quad \text{(A1-6a)}$$

$$\int_{-\infty}^{+\infty} G(x, y, 0, y')\,dy' = \frac{d_0}{\epsilon_2} = \frac{1}{C_0} \quad \text{(A1-6b)}$$

$$\int_{-\infty}^{+\infty} G(0, y, x', y')\,dy' = \frac{d_0}{\epsilon_2} = \frac{1}{C_0} \quad \text{(A1-6c)}$$

$$\int_{-\infty}^{+\infty} \frac{\partial G}{\partial y}(x, y, x', y')\,dy' = 0 \quad \text{(A1-6d)}$$

where C_0 is the insulator capacity per unit area. In the case when $q(y)$ is a constant, using (A1-4)–(A1-6), the surface potential is given by

$$\Phi_s = V_G + \frac{q}{C_0} + \frac{eN_DX_D}{C_0} \quad \text{(A1-7a)}$$

$$V_G + \frac{q}{C_0} + \frac{eN_DX_D}{C_0} - \frac{eN_DX_D^2}{2\epsilon_1} = 0. \quad \text{(A1-7b)}$$

Equations (A1-7a) and (A1-7b) are the one-dimensional solutions of the Poisson equation using the depletion approximation for the MIS structure [33]. For a given surface-charge density profile, the surface-potential gradient can be obtained according to the gradual channel

approximation by differentiating (A1-7a)

$$\frac{\partial \Phi_s}{\partial y} = \frac{1}{C_0}\frac{\partial q}{\partial y} + \frac{eN_D}{C_0}\frac{\partial X_D}{\partial y}. \quad \text{(A1-8)}$$

A more accurate estimation of the surface-potential gradient can be obtained from (A1-4) and (A1-6).

$$\frac{\partial \Phi_s}{\partial y} = \int_{-\infty}^{+\infty} \frac{\partial G}{\partial y}(0, y, 0, y')q(y')\,dy' + \int_{-\infty}^{+\infty} dy' \int_0^{X_D(y')} \frac{\partial G}{\partial y}(0, y, x', y')eN_D\,dx'. \quad \text{(A1-9)}$$

The first term in (A1-9) represents the repulsive force due to the nonuniform surface charge $q(y)$, screened by the metal electrode. The second term represents the repulsive force from the ionized fixed impurity atoms due to the nonuniform depletion region thickness. Let us consider the first term from (A1-3)

$$\frac{\partial G}{\partial y}(0, y, 0, y') = \frac{-1}{\pi(\epsilon_1 + \epsilon_2)}\left\{\frac{1}{y - y'} - \frac{2\epsilon_2}{(\epsilon_1 + \epsilon_2)} \cdot \sum_{m=1}^{\infty}\left(\frac{\epsilon_1 - \epsilon_2}{\epsilon_1 + \epsilon_2}\right)^{m-1} \frac{(y - y')}{(y - y')^2 + (2md_0)^2}\right\}. \quad \text{(A1-10)}$$

For the silicon oxide, silicon substrate

$$\frac{2\epsilon_2}{\epsilon_1 + \epsilon_2} \cong \tfrac{1}{2}$$

$$\frac{\epsilon_1 - \epsilon_2}{\epsilon_1 + \epsilon_2} \cong \tfrac{1}{2}.$$

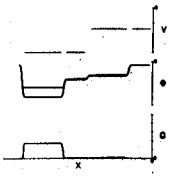
Thus the successive terms in the previous series decrease rapidly. So the Green's function $(\partial G/\partial y)$ decreases rapidly within a region of a few d_0 from y, however not as rapid as it would be if $\epsilon_2 = \epsilon_1$. Hence, we may expand $q(y')$ as a Taylor series about y. Since $(\partial G/\partial y)$ is odd, all even terms in the expansion vanish. If the variation of the surface charge $q(y)$ is small over a distance on the order of a few oxide thickness d_0, $(\partial^3 q(y')/\partial y'^3)$ and higher derivatives may be neglected. Hence,

$$\int_{-\infty}^{+\infty} \frac{\partial G}{\partial y}(0, y, 0, y')q(y')\,dy' = +\frac{\partial q}{\partial y}\int_{-\infty}^{+\infty} G(0, y, 0, y')\,dy' = \frac{\partial q}{\partial y}\frac{1}{C_0}. \quad \text{(A1-11)}$$

This is the result obtained in the first term of the one-dimensional solution in (A1-8). So if the variation of the depletion layer width is neglected, the surface-potential gradient obtained by differentiating the one-dimensional solution in (A1-7a) includes the charge repulsion effect, and gives a reasonably accurate estimate of the self-induced fields when the lateral variation of the surface-charge density over a distance on the order of several oxide thickness is small. The error in this estimate depends upon the charge profile and may be positive or negative.

Similarly the contribution of the second term in (A1-9) can be shown to be almost equal to the value obtained from the second term of the one-dimensional solution in (A1-8) when the lateral variation of the charge over a distance on the order of the depletion region thickness is small.

The surface-charge density profiles under the CCD gates, show that, during the charge transfer, the surface-charge density varies slowly under the electrodes but rapidly in the interelectrode regions. So the gradual channel approximation gives accurate estimates of the self-induced fields under the electrodes. As discussed in Sections III and IV, the charge transfer in all stages is limited by the transfer of charge across the transfer gates or out of the storage gate. Hence, the error in estimating the self-induced fields in the interelectrode regions has a negligible effect on the overall charge-transfer characteristics.



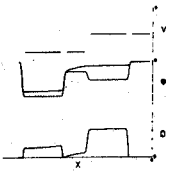
Appendix II

Derivation of the Surface-Potential Gradient Under the Gate Electrodes and in the Interelectrodes Regions

The one-dimensional solution of the Poisson equation using the depletion approximation gives the following relation between the surface-potential ϕ_s, and the surface-charge density [1] q:

$$\Phi_s = V_G - V_{FB} + \frac{q}{C_0} + \frac{B}{C_0} \cdot \left[\sqrt{1 - 2\frac{C_0}{B}\left(V_G - V_{FB} + \frac{q}{C_0}\right)} - 1\right], \quad \text{(A2-1)}$$

where $B = \epsilon_s/(\epsilon_{ox})eN_D d_0 \cdot V_G$ is the voltage applied to the electrode, V_{FB} is the flat-band voltage, C_0 the oxide capacitance per unit area, e the electronic charge, N_D the donor concentration, d_0 the oxide thickness, and X_d the width of the depletion region. ϵ_s and ϵ_{ox} are the dielectric constants of silicon and silicon oxide, respectively. The equilibrium surface-charge density q_0 is equal to $C_0(V_{Th} - V_G)$, where V_{Th} is the threshold voltage. If the surface-charge profile q is not uniform then according to the gradual channel approximation, the surface-potential gradient is given approximately by



$$\frac{\partial \Phi_s}{\partial x} = \frac{\partial \Phi_s}{\partial q}\frac{\partial q}{\partial x} = \frac{\partial q/\partial x}{C_0 + C_D} = \frac{1}{C_0}\left[1 - \frac{1}{\sqrt{1 - 2\frac{C_0}{B}\left(V_G - V_{FB} + \frac{q}{C_0}\right)}}\right]\frac{\partial q}{\partial x} \quad \text{(A2-2)}$$

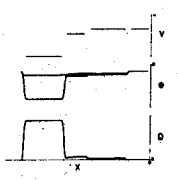
where C_D is the depletion layer capacity. For typical oxide thickness, (~1000–4500 A), substrate doping (~10^{14}–10^{16}/cm^3) and electrode voltages the previous relations can be simplified to

$$\Phi_S = \Phi_{S0} + \frac{q}{C}$$

and

$$\frac{\partial \Phi_S}{\partial x} = \frac{1}{C}\frac{\partial q}{\partial x}, \quad \text{(A2-3)}$$

where Φ_{S0} is the surface potential with no charge. C is an effective capacity given by



$$C = \frac{q_0 \cdot F}{(2\Phi_F - \Phi_{S0})}, \quad \text{(A2-4)}$$

where $2\Phi_F$ the surface potential at equilibrium, and F a factor less than unity to reduce the error in this approximation to less than few percents.

Numerical calculations using values of the self-induced fields given in (A2-2) and (A2-3) show almost no difference in the charge-transfer characteristics. Since the latter expression is simpler, we will use it below.

If fringing fields under the electrodes are appreciable, then Φ_{s0} and q_0 are functions of time and the spatial coordinate x and are given by

$$\Phi_{s0}(x, t) = \Phi_{s0}(t) - \int_x E_{fr}(y)\, dy \tag{A2-5}$$

$$q_0(x, t) = C_0\{[2\Phi_F - \Phi_{s0}(x, t)] + \sqrt{2\epsilon_s e N_D}\,[\sqrt{|\Phi_{s0}(x, t)|} - \sqrt{|2\Phi_F|}]\} \tag{A2-6}$$

where $E_{fr}(y)$ is the fringing-field profile obtained from the solution of the two-dimensional Poisson equation and $\Phi_{s0}(t)$ is given by (A2-1) with $q = 0$. The surface potential under the electrode is thus given by

$$\Phi_s(x, t, q) = \Phi_{s0}(x, t) + \frac{(2\Phi_F - \Phi_{s0}(x, t))q}{q_0(x, t)F}. \tag{A2-7}$$

In the interelectrode regions the surface potential is also given by

$$\Phi_S(x, t, q) = P(x, t) + \frac{(2\Phi_F - P(x, t))q}{C(x, t)} \tag{A2-8}$$

where $P(x, t)$ and $C(x, t)$ are the surface potential with no charge and the equilibrium surface-charge density, respectively, both approximated by a smooth interpolating polynomial. From (A2-7) and (A2-8) the surface-potential gradient under the electrodes and the interelectrode regions can be written in the following form

$$\frac{\partial \Phi_S}{\partial x}(x, t, q) = L(x, t) + M(x, t)q + N(x, t)\frac{\partial q}{\partial x}. \tag{A2-9}$$

Appendix III
Steady-State Current and Charge Under the Transfer Gate

Assuming that the charge redistribution time under the transfer gate is much smaller than the transfer times of interest, then the current across it and the charge under it can be approximately derived by a steady-state approach.

The relation between the surface potential and surface-charge density under the transfer gate according to the gradual channel approximation is given by

$$\Phi_T = \Phi_{T0} + \frac{q}{C_{tr}}, \tag{A3-1}$$

where Φ_T and Φ_{T0} are the surface potential under the transfer gate with charge and with no charge, respectively, q is the mobile surface-charge density, C_{Tr} the effective oxide and depletion layer capacity under the transfer gate. The current I under the transfer gate is given by

$$I = W\left(-D\frac{\partial q}{\partial x} - \mu q\frac{\partial \Phi_T}{\partial x}\right) \tag{A3-2}$$

where D and μ are the surface diffusion constant and mobility, respectively, and W is the channel width. If fringing fields under the transfer gate are neglible (A3-2) may be rewritten as

$$I = -W\mu C_{Tr}\left[KT\frac{\partial \Phi_T}{\partial x} + (\Phi_T - \Phi_{T0})\frac{\partial \Phi_T}{\partial x}\right], \tag{A3-3}$$

where KT is the thermal voltage.

If we let the surface potential at the beginning and end of the transfer be Φ_T and Φ_T', then assuming the current I across the gate constant and integrating (A3-3) we get

$$I = \frac{\mu C_{Tr} W}{2l_{Tr}}[2KT(\Phi_T - \Phi_T') + (\Phi_T - \Phi_T')(\Phi_T + \Phi_T' - 2\Phi_{T0})], \tag{A3-4}$$

and

$$Q_{Tr} = \tfrac{2}{3} l_{Tr} W C_{Tr}(\Phi_T - \Phi_{T0}) \cdot \frac{\left\{(\Phi_T - \Phi_{T0}) + \tfrac{3}{2}KT + (\Phi_T' - \Phi_{T0})\left[1 + \frac{\tfrac{3}{2}KT}{(\Phi_T - \Phi_{T0})} + \frac{(\Phi_T' - \Phi_{T0})}{(\Phi_T - \Phi_{T0})}\right]\right\}}{\{(\Phi_T - \Phi_{T0}) + (\Phi_T' - \Phi_{T0}) + 2KT\}} \tag{A3-5}$$

where l_{Tr} is the length of the transfer gate and Q_{Tr} is the total charge under the transfer gate.[18] In the case the surface-charge density at the end of the transfer gate is very small (as in the two-phase clocking scheme) then $\Phi_T' \approx \Phi_{T0}$ and (A3-4) and (A3-5) reduce to

$$I = \frac{\mu C_{Tr} W}{2l_{Tr}}[(\Phi_T - \Phi_{T0})^2 + 2KT(\Phi_T - \Phi_{T0})] \tag{A3-6}$$

$$Q_{Tr} = \tfrac{2}{3} l_{Tr} W C_{Tr}(\Phi_T - \Phi_{Tr})\frac{[(\Phi_T - \Phi_{T0}) + \tfrac{3}{2}KT)]}{[(\Phi_T - \Phi_{T0}) + 2KT]}. \tag{A3-7}$$

If $(\Phi_T - \Phi_{T0}) \gg KT$, (A3-6) and (A3-7) reduce further to

$$I = \frac{\mu C_{Tr} W}{2l_{Tr}}(\Phi_T - \Phi_{T0})^2 \tag{A3-8}$$

$$Q_{Tr} = \tfrac{2}{3} l_{Tr} W C_{Tr}(\Phi_T - \Phi_{T0}). \tag{A3-9}$$

The current formula in (A3-8) is the quadratic relation of the MOS transistor at pinchoff, and the factor $\frac{2}{3}$ in (A3-9) is due to the square root dependence of the surface-charge density q on the distance from the end of the transfer gate.

If $(\Phi_T - \Phi_{T0}) < 2KT$, then the charge transport under the transfer gate is mainly by diffusion, and the previous equations reduce to

$$I = \frac{\mu C_{Tr} W}{l_{Tr}}(KT)(\Phi_T - \Phi_{T0}) = \frac{C_{Tr} W D}{l_{Tr}}(\Phi_T - \Phi_{T0}). \tag{A3-10}$$

$$Q_{Tr} = \tfrac{1}{2} l_{Tr} W C_{Tr}(\Phi_T - \Phi_{T0}). \tag{A3-11}$$

The factor $\frac{1}{2}$ in (A3-11) is due to the linear dependence of the surface-charge density q on the distance from the end of the transfer gate.

If the fringing fields under the transfer gates are appreciable then the previous current relations still hold approximately after replacing KT and (D/l_{Tr}) by $(KT + l_{Tr}\bar{E})$ and $(D/l_{Tr} + \mu\bar{E})$, respectively, where $\bar{E}$ is the average fringing field weighted by the surface-charge density profile under the transfer gate.

[18] Note that the last term in (A3-5) is a very slowly varying function taking a value between $\frac{3}{4}$ and $\frac{3}{2}$ depending on the value of $(\Phi_{mT} - \Phi_{mT0})$ and $(\Phi_{mT}' - \Phi_{mT0}')$. So taking the value of this term unity is a good approximation to simplify the solution of the differential equation (A4-5) for any clocking waveforms.

Appendix IV
Lumped-Circuit Model of CCD's

The detailed numerical solution of the transport dynamic with various clocking waveforms show that during the different stages of the charge-transfer process the surface-charge profiles under the gates take almost a steady shape. The response time of the charge distribution under the gates is of the order of the dielectric relaxation time of the surface minority carrier [33]. During all the stages of the charge transfer the surface-charge density is sufficiently large that the response time is orders of magnitude smaller than the transfer times of interest. Hence, it is possible to describe approximately the details of the charge-transfer dynamics with various clocking waveforms by means of a lumped-circuit model that consists of lumped capacitors charged and discharged through lumped-transfer channels (MOS transistors).

As discussed in Sections III and IV in the first stages of the charge-transfer process, the rate of charge transfer is limited by the transport of charge across the transfer gate and depends strongly on the clocking waveforms. Due to the relatively large carrier concentration under the storage gates, a very small gradient in the quasi-Fermi level E_f under the storage gates is sufficient to balance the discharge current. Thus the surface potential and the mobile carrier concentration under the storage gates are almost constant. So the total charge under the source and receiving storage gate Q_{St} and Q_{st}' are given by $Wl_{St}C_{St}(\Phi_s - \Phi_{s0})$ and $Wl_{St}C_{St}(\Phi_s' - \Phi_{s0}')$, respectively, where the surface potential with and without charge, under the source storage gate are Φ_S and Φ_{S0} and under the receiving storage gate are Φ_S' and Φ_{S0}', respectively. The transfer gate acts as a MOS transistor with the source and receiving storage gates as its source and rain. The quasi-Fermi level may be assumed constant across the transitional region between the source storage gate and the transfer gate during the first stages of the charge-transfer process as this region extends over several times the mean carrier freepath and the mobile carrier concentration there is relatively large. Therefore the surface potential at the end of the source storage gate Φ_S is related to the surface potential at the beginning of the transfer gate Φ_T by

$$C_{Tr}(\Phi_T - \Phi_{T0}) = C_{St}(\Phi_S - \Phi_{S0}) \exp\left(-(\Phi_T - \Phi_S)/KT\right) \tag{A4-1}$$

and

$$\left[1 + \frac{KT}{\Phi_T - \Phi_{T0}}\right] \cdot \frac{d}{dt}(\Phi_T - \Phi_{T0}) = \left[1 + \frac{KT}{\Phi_S - \Phi_{S0}}\right] \cdot \frac{d}{dt}(\Phi_s - \Phi_{s0}) + \frac{d}{dt}(\Phi_{S0} - \Phi_{T0}^{*}). \tag{A4-2}$$

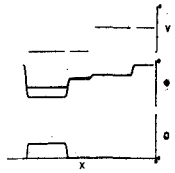
Φ_T and Φ_{T0} are the surface potential under the beginning of the transfer gate with and without charge. For $(\Phi_T - \Phi_{T0}) \gg KT$ and $(\Phi_S - \Phi_{S0}) \gg KT$ the previous equations reduce to

$$\Phi_T \cong \Phi_S \tag{A4-3}$$

and

$$\frac{d}{dt}(\Phi_T - \Phi_{T0}) = \frac{d}{dt}(\Phi_S - \Phi_{S0}) + \frac{d}{dt}(\Phi_{S0} - \Phi_{T0}). \tag{A4-4}$$

If the mobile carrier concentration in the transitional region between the transfer gate and the receiving storage gate is also relatively large (as in the four-phase clocking scheme) then the surface potential at the end of the transfer gate Φ_T' is related to the surface potential at the beginning of the receiving storage gate Φ_S' by similar relations. The total charge under the transfer gate Q_{Tr} and the current I across it are given by (A3-5) and (A3-4). So, according to this lumped-circuit model, the total charges under the storage and transfer gates are related to the surface potentials by lumped capacitors of almost constant values that are charged and discharged through lumped-transfer channels with discharge current that depend mainly on the difference between the surface potential at the ends of the transfer channels. The charge-transfer dynamics could be simply described by a first order nonlinear differential equation given by



$$\frac{d}{dt}(Q_{St} + Q_{Tr}) = -I(\Phi_T, \Phi_T', \Phi_{T0}) \tag{A4-5a}$$

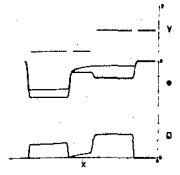
$$Q_{St} \cong Wl_{St}C_{St}(\Phi_S - \Phi_{S0}) \tag{A4-5b}$$

$$Q_{St}' \cong Wl_{St}C_{St}(\Phi_S' - \Phi_{S0}') = Q_0 - Q_{St} - Q_{Tr} \tag{A4-5c}$$

$$Q_{Tr} \cong \tfrac{2}{3}Wl_{Tr}C_T(\Phi_T - \Phi_{T0}) \tag{A4-5d}$$

$$\Phi_T \cong \Phi_S, \qquad \Phi_T' \cong \Phi_S' \tag{A4-5e}$$

$$I(\Phi_T, \Phi_T', \Phi_{T0}) = \frac{\mu C_{Tr}W}{2l_{Tr}}\left[2KT(\Phi_T - \Phi_T') + (\Phi_T - \Phi_T')(\Phi_T + \Phi_T' - 2\Phi_{T0})\right] \tag{A4-5f}$$



where KT is the thermal voltage and Q_0 is the initial total charge. Φ_{T0}, Φ_{S0}, and Φ_{S0}' depend on the clock voltage waveforms. In the two-phase clocking scheme, there is usually a large surface-potential gradient between the transfer gate and the receiving storage gate. The transfer gate thus acts as an MOS transistor at pinchoff and $\Phi_T' \cong \Phi_{T0}$. In this case the current I and the total charge under the transfer gate Q_{Tr} are given by (A3-6) and (A3-7). The solutions of the charge-transfer characteristics using the lumped-circuit model for a two-phase drop clock with zero fall and rise times and for a two-phase push clock discussed in Section III, give good agreement with the numerical solution of the transport equations given in (5).

During the last stages of the charge transfer, when the device is operated in the complete charge-transfer mode, the charge transfer is limited by the transport of charge out of the storage gate with an almost perfect sink at its end. In this case also the storage gate can be considered as a capacitor discharged through a transfer channel which is the same storage gate. Assuming a constant steady current across the storage gate, the total charge under it Q_{St} and the discharge current I are given by (A3-6) and (A3-7), respectively. Solving the discharge equation $I = -(d/dt)Q_{St}$ gives approximately

$$\frac{Q_{St}}{Q_0} = \frac{\exp\left(-(t - t_3)/\tau\right)}{1 + \dfrac{Q_0}{\frac{2}{3}C_{St}l_{St}W}\dfrac{1}{2KT}\left[1 - \exp\left(-(t - t_3)/\tau\right)\right]}, \tag{A4-6}$$

where $\tau = l_{St}^2/2D$ and Q_0 is the initial total charge under

the gate when this stage of the charge-transfer process starts at time t_3.

The assumption of a constant steady current across the storage gate is expected to be reasonably good when the nonlinear terms due to the self-induced fields are dominant. But since the effects of the boundary conditions, the fringing fields, the shape of the mobile carrier concentration profile under the gates are not properly considered in the previous derivation, the time constant τ of the exponential decay of the charge should be modified. Analytic solutions of the charge transport dynamics including thermal diffusion and fringing-field drift only with the appropriate boundary conditions show that the final decay time constant τ is given approximately [21] by

$$\frac{1}{\tau_f} = \frac{4}{\tau_d} + \frac{(\mu E_{\min})^2}{4D} \tag{A4-7}$$

where $E_{\min}$ is the minimum fringing field under the storage gate, τ_d is the thermal diffusion time constant and is equal to $(4l_{St}^2/\pi^2 D)$. The factor 4 in front of the second term is due to the large fields at the edges of the gate, and for zero fringing field this factor takes a value of unity. Accordingly (A4-6) could be modified to

$$\frac{Q_{St}}{Q_0} = \frac{\exp\left(-(t-t_3)/\tau_f\right)}{1 + \dfrac{Q_0}{\frac{2}{3}C_{St}l_{St}W}\cdot\dfrac{1}{2KT}\cdot\dfrac{\tau_f}{\tau_d}\left[1 - \exp\left(-t-t_3\right)/\tau_f\right)\right]}. \tag{A4-8}$$

The factor τ_f/τ_d in the denominator is included in order not to modify the original equation for $(t - t_3) < \tau_f$, as the effect of the fringing-field drift is expected to be smaller than the self-induced drift in this period.

Using (A3-6) and (A3-7) the charge under the transfer gate is described approximately by

$$\frac{dQ_{T_r}}{dt} + \frac{\mu C_{T_r}W}{2l_{T_r}}\frac{Q_{T_r}}{\frac{1}{2}C_{T_r}l_{T_r}W} \cdot\left[2(l_{T_r}\bar{E} + KT) + \frac{Q_{T_r}}{\frac{1}{2}C_{T_r}l_{T_r}W}\right] = -\frac{dQ_{St}}{dt} \tag{A4-9}$$

where $\bar{E}$ is the average fringing field weighted by the surface-charge density profile under the transfer gate. Using Ricatti's substitution, this equation could be solved by the WKB method [28]. However, an approximate solution can be obtained in the overlapping gates structures as the transfer gates are usually shorter and have larger fringing fields than the storage gates. So the carriers are swept rapidly from under the transfer gate and for transfer time of practical interest, the solution simplifies to

$$Q_{T_r} \cong \tau_{T_r}\left(-\frac{dQ_{St}}{dt}\right) \tag{A4-10}$$

where τ_{T_r} is the single-carrier transit time under the transfer gate and is given by $\tau_{T_r} = [l_{T_r}^2/2\mu(KT + \bar{E}l_{T_r})]$.

Acknowledgment

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References

[1] W. S. Boyle and G. E. Smith, "Charge-coupled semiconductor devices," *Bell Syst. Tech. J.*, vol. 47, pp. 587–592, Apr. 1970.

[2] M. F. Tompsett, G. F. Amelio, and G. E. Smith, "Charge-coupled 8-bit shift register," *Appl. Phys. Lett.*, vol. 17, pp. 111–115, 1970.

[3] C. K. Kim and E. H. Snow, "p-channel charge-coupled devices with resistive gate structure," *Appl. Phys. Lett.*, vol. 20, pp. 514–516, 1972.

[4] W. Engeler, J. J. Tiemann, and R. D. Baertsch, "Surface charge transport in silicon," *Appl. Phys. Lett.*, vol. 17, pp. 469–472, 1970.

[5] W. F. Kosonocky and J. E. Carnes, "Charge-coupled digital circuits," *IEEE J. Solid-State Circuits*, vol. SC-6, pp. 314–326, Oct. 1971.

[6] N. G. Vogl and T. V. Harroun, "Operating memory system using charge-coupled devices," in *ISSCC Dig. Tech. Papers*, Feb. 1972, p. 246.

[7] C. K. Kim and M. Lenzlinger, "Charge transfer in charge-coupled devices," *J. Appl. Phys.*, vol. 42, pp. 3586–3594, 1971.

[8] R. J. Strain and N. L. Shryer, "A nonlinear diffusion analysis of charge-coupled device transfer," *Bell Syst. Tech. J.*, vol. 50, pp. 1721–1740, July/Aug. 1971.

[9] J. E. Carnes, W. F. Kosonocky, and E. G. Ramberg, "Free charge transfer in charge-coupled devices," *IEEE Trans. Electron Devices*, vol. ED-19, pp. 798-808, June 1972.

[10] G. F. Amelio, "Computer modeling of CCD characteristics," *Bell Syst. Tech. J.*, vol. 51, 1972.

[11] L. G. Heller, W. H. Chang, and A. W. Lo, "A model of charge transfer in bucket brigade and charge-coupled devices," *IBM J. Res. Develop.*, vol. 16, pp. 184–187, Mar. 1972.

[12] H.-S. Lee and L. G. Heller, "Charge-control method of charge-coupled device transfer analysis," *IEEE Trans. Electron Devices*, vol. ED-19, pp. 1270–1279, Dec. 1972.

[13] C. N. Berglund, "Analog performance limitations of charge transfer dynamic shift registers," *IEEE J. Solid-State Circuits*, vol. SC-6, pp. 391–396, Dec. 1971.

[14] H. B. Keller, *Numerical Solutions of Partial Differential Equations*, vol. 2. New York: Academic Press, 1971, p. 327.

[15] A. M. Mohsen, T. C. McGill, Y. Daimon, and C. A. Mead, "The influence of interface states in incomplete charge transfer in overlapping gate charge-coupled devices," *IEEE J. Solid-State Circuits*, vol. SC-8, pp. 125–138, Apr. 1973.

[16] A. M. Mohsen, T. C. McGill, and C. A. Mead, "Charge transfer in charge-coupled devices," in *ISSCC Dig. Tech. Papers*, vol. 15, pp. 248–249, 1972.

[17] ——, "Influence of clocking waveforms on charge transfer in charge-coupled devices," presented at the 1972 Electron Devices Meeting, Edmonton, Alta., Canada, June 21–23, 1972, to be published.

[18] A. M. Mohsen, Ph.D. dissertation, California Institute of Technology, Pasadena.

[19] C. N. Berglund and R. J. Strain, "Fabrication and performance consideration of charge-transfer dynamic shift registers," *Bell Syst. Tech. J.*, vol. 51, pp. 655–703, 1972.

[20] S. M. Sze, *Physics of Semiconductor Devices*. New York: Wiley, 1969, p. 517.

[21] Y. Daimon, A. M. Mohsen, T. C. McGill, and C. A. Mead, to be published.

[22] O. Leistiko, A. S. Grove, and C. T. Sah, "Electron and hole mobilities in inversion layers on thermally oxidized surfaces," *IEEE Trans. Electron Devices*, vol. ED-12, pp. 248–254, May 1965.

[23] J. F. Gibbons, "Papers on carrier drift velocities in silicon at high electric field strengths," *IEEE Trans. Electron Devices*, vol. ED-14, pp. 3–7, Jan. 1967.

[24] R. H. Krambeck, R. H. Walden, and K. A. Pickar, "Implanted barrier two-phase charge-coupled devices," *Appl. Phys. Lett.*, vol. 19, pp. 502–522, Dec. 1971.

[25] C. A. T. Salama, "Two phase MNOS charge-coupled device," *Electron. Lett.*, vol. 8, pp. 21–22, Jan. 1972.

[26] A. M. Mohsen, T. C. McGill, M. Anthony, and C. A. Mead, "Dynamic push clock, A new approach to charge-coupled device clocking," *Appl. Phys. Lett.*, vol. 22, pp. 172–175, Feb. 15, 1973.

[27] A. M. Mohsen, M. Anthony, W. Watrous, and C. A. Mead, unpublished.

[28] L. R. Ford, *Differential Equations*. New York: McGraw-Hill, 1933, p. 40.

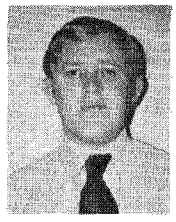
[29] K. K. Thornber, "Incomplete charge transfer in IGFET bucket-brigade shift registers," *IEEE Trans. Electron Devices*, vol. ED-18, pp. 941–950, Oct. 1971.

[30] W. G. Engeler, J. J. Tiemann, and R. D. Baertsch, "A memory system based on surface-charge transport," in *ISSCC Dig. Tech. Papers*, 1971, pp. 164–165.

[31] S. R. Hofstein, "Minority carrier lifetime determination from inversion layer transient response," *IEEE Trans. Electron Devices*, vol. ED-14, pp. 785–786, Nov. 1971.

[32] J. H. Jeans, *The Mathematical Theory of Electricity and Magnetism*: New York: Cambridge Univ. Press.
[33] A. S. Grove, B. E. Deal, E. H. Snow, and C. T. Sah, "Investigation of thermally oxidized silicon surfaces using metal-oxide-semiconductor structures," *Solid-State Electron.*, vol. 8, p. 145, 1965.
[34] S. R. Hofstein and G. Warfield, "Physical limitations on the frequency response of a semiconductor inversion layer," *Solid-State Electron.*, vol. 8, pp. 321–341, 1965.

Amr M. Mohsen, for a photograph and biography, please see page 188 of the April 1973 issue of this JOURNAL.



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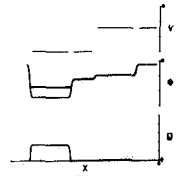

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Bucket-Brigade Shift-Register Operation–Exact Correlation Between Experimental Data and a Computer Model

E. T. LEWIS

Abstract—**In this paper a detailed analysis of the IGFET bucket brigade is presented covering its low frequency, midfrequency, and high frequency performance. Attention is first focused on those factors giving rise to performance limits in the midfrequency range of operation. The concept of an optimized threshold voltage V_{TO} is introduced and related to the array parameters. It is shown that if the threshold voltage V_T of the IGFET's in the array are below V_{TO}, then transfers become incomplete. The effect that substrate resistivity has on the array performance is also considered. It is shown that conventional IGFET channel length modulation is not the only factor to be considered in analyzing this performance limit. It is also shown that high frequency and low frequency limits can be accounted for using conventional IGFET theory.**

Finally, calculations resulting from a simple model that includes all these effects are presented. They are shown to correlate exactly with the experimental data from operating arrays.

I. Introduction

THE bucket-brigade shift register has been investigated in some detail by a number of people [1]–[8]. However, to date, there has been little attempt to consolidate the growth in accumulated data. Even more important, there has been no attempt to give an explicit analysis of the low frequency, midfrequency, and high frequency performance of an integrated array illustrating all the interdependencies that exist between operating conditions and the array parameters. Such an analysis is necessary if it is desired to seek optimum design and, hence, optimum performance of bucket-brigade shift registers.

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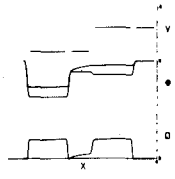
In the analysis to be presented here we begin from a quasi-static position (midfrequency) illustrating all the basic parameter interdependencies, and then proceed to include the factors affecting the low frequency and high frequency performance. This analysis has been confirmed by experiment using a relatively complex integrated test vehicle and a computer model that incorporates all the physical parameters of an integrated array. In addition to measurements performed on integrated arrays some data were obtained on single elements to demonstrate and quantify basic effects associated with an IGFET. The results of these measurements were important in that they aided in explaining some of the effects observed in the integrated bucket-brigade array.



II. Description and Basic Operation of an Integrated Bucket-Bridgade Shift Register

The basic elements of a p-channel IGFET bucket brigade are shown in Fig. 1. In the electrical equivalent shown in Fig. 1(b) are included node-loading elements and an output precharge device. The node-loading elements can represent either junction capacitance or a combination of this capacitance and that of input/output devices. In some applications it is desired to have serial input to the array and parallel output from every storage node. Actually, there are many combinations of input/output arrangements for which bucket brigades can be designed. These include serial in-serial out, serial in-parallel out, parallel in-serial out, and parallel in-parallel out. In addition to this any of these arrangements can be operated in a recirculation mode. This permits a dynamic storage mode of operation in which